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PATENT & TRADEMARK OFFICE

Docket No. A1WI2376US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Douglas W. Babcock, Robert A. Duris,
Bruce Recht

Serial No. 10/722,970

Filed: November 25, 2003

Title: AUTOMATIC TEST EQUIPMENT PIN CHANNEL WITH
T-COIL COMPENSATION

Commissioner for Patents
Mail Stop Amendment
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF ROBERT A. DURIS

I, Robert A. Duris, declare:

1. I am a co-inventor of the invention which is the subject of the above-identified patent application.
2. At all times mentioned herein I was, and am presently, a Senior Staff Engineer for Analog Devices, Inc. (ADI), the assignee of the invention and patent application.
3. Attached as Exhibit 1 is a copy of a slide presentation I gave on April 13, 2000 at the annual ADI General Technical Conference, entitled "Integrated Bridged T-Coils for ATE Pin Electronics". This is an internal conference within ADI intended to brief employees on new developments within the company that have not yet become public. My presentation was confidential to ADI, and the slides were marked "ADI Proprietary." The slides documented

Best Available Copy

my concept of the invention, and disclosed the invention as claimed in the application.

4. Attached as Exhibit 2 is an annotated copy of selected figures from Exhibit 1, marked up as follows to show the correspondence between the figure elements and the elements of the application claims:

Page 2: This figure illustrates a bridged T-Coil circuit that can be used for the "passive matching network" of the claims, as described in the specification at page 9, line 30-page 10, line 7.

Page 4: This figure illustrates the problem which the invention addresses, with a circuit that includes the "ATE bidirectional drive channel", "device under test (DUT)", "input/output line for connection to a DUT", "driver circuit", "receiver circuit" and "associated capacitance" of the receiver circuit recited in claim 1 of the application, but not the passive matching network of claim 1.

Page 6: This figure is similar to the page 4 figure up to the DUT, but shows the addition of the "first passive matching network" to at least partially compensate for receiver circuit capacitance connected to the input/output line of claim 1. The "passive matching network" is shown implemented as a "T-coil circuit" as in claim 2. Instead of the single driver circuit on page 4, it shows the driver circuit implemented as the combination of current-mode and voltage-mode driver circuits as in claim 5.

Page 7: This figure is similar to the page 6 figure, but instead of the simple "passive matching network" on page 6 it shows two passive matching networks as in claim 5, with the second passive matching network "connected in series with the first passive matching network to at least partially compensate for the current-mode driver capacitance" as in claim 5. Both passive matching networks are shown implemented as respective T-coils, as in claim 6.

Page 10: This figure illustrates the T-coil circuit including "inductors that are implemented in a separate layer" of an integrated circuit (IC) that is spaced by at least a dielectric layer from a "common layer" on which the driver and receiver circuits are implemented, as in claim 3.

Page 40: This page displays a photograph of a chip layout to implement the invention as claimed in claims 1, 5 and 6, discussed above.

5. On May 25, 2000 a circuit design to implement the invention was released to the ADI fabrication facility. Attached as Exhibit 3 is a copy of IC chip layouts dated May 23, 2000, marked-up to show the claimed elements of the invention, including T-coil circuits that were internal to the chip and implemented in its metal-3 layer.

6. On August 22, 2000 a first wafer lot was received from the ADI fabrication facility, and on September 15, 2000 a second wafer lot was received. The second lot had

the same functional circuitry as the first lot, but the location of connection vias was changed to allow for the addition of post-passivation T-coils external to the chip. The internal T-coils implemented in the metal-3 layer were of aluminum approximately three microns thick, whereas post-passivation T-coils were of copper or gold up to ten microns thick. It was believed that internal T-coils would be functional, but that post-passivation T-coils would perform better. Exhibit 4 is a copy of a test trace that was obtained from the wafer received August 22, 2000, performed the same day, showing that both the current-mode driver (A) and the voltage-mode driver (AB) were functional.

7. The development of test software to test the second T-coil wafer lot began on September 15, 2000 when the wafer lot was received, and was completed on September 20, 2000. On the latter date the circuits on the second wafer lot were tested; a printout of the test results is appended as Exhibit 5. Of the 95 circuits tested, 24 had metal-3 T-coils. The test results are summarized on the first page of Exhibit 5. The last line of this page indicates a yield of 17/24 for the metal-3 T-coils circuits, meaning that 17 of the 24 circuits tested worked properly. Only DC testing was performed at this time, which did not show whether the T-coil circuits successfully compensated for the receiver circuit capacitance. The testing was performed by Daniel Sheehan, an ADI employee.

8. On September 20, 2000 the second lot wafers were sent to Advanced MicroSensors, Inc., an independent

company, for the addition of post-passivation T-coils. The completed wafers, including post-passivation T-coils, were returned to ADI on October 12, 2000. A copy of the Advanced MicroSensors cover letter transmitting the completed wafers is attached as Exhibit 6. Copies of photographs taken by Advance MicroSensors of the post-passivation T-coils are attached as Exhibit 7.

9. Beginning upon the receipt of the post-passivation T-coil wafers on October 12, 2000, ADI developed a characterization setup in its characterization laboratory to test and characterize the drive channel circuits to which Advanced MicroSystems had added post-passivation T-coils. A circuit with the post-passivation T-coils was tested on October 17, 2000, and a copy of a trace of the results is attached as Exhibit 8, plotting ρ as a function of time. ρ is a measure of impedance matching; the results show a negative peak of about -120mp. A similar circuit but without post-passivation T-coils was tested on October 18, 2000, and a copy of a trace of the results is attached as Exhibit 9. This trace shows a negative peak of about -260mp, which indicated that the addition of the post-passivation T-coils was successful in substantially compensating the receiver circuit capacitance. Both tests were made by Robert Bombara, an ADI employee.

10. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge

that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: May 30, 2006



Robert A. Duris

(U/MA/B88/abond/b, ac Robert A. Duris 11/23/2005)

Integrated Bridged T-Coils for ATE Pin Electronics

Presented by

Bob Duris

ATE Products Group

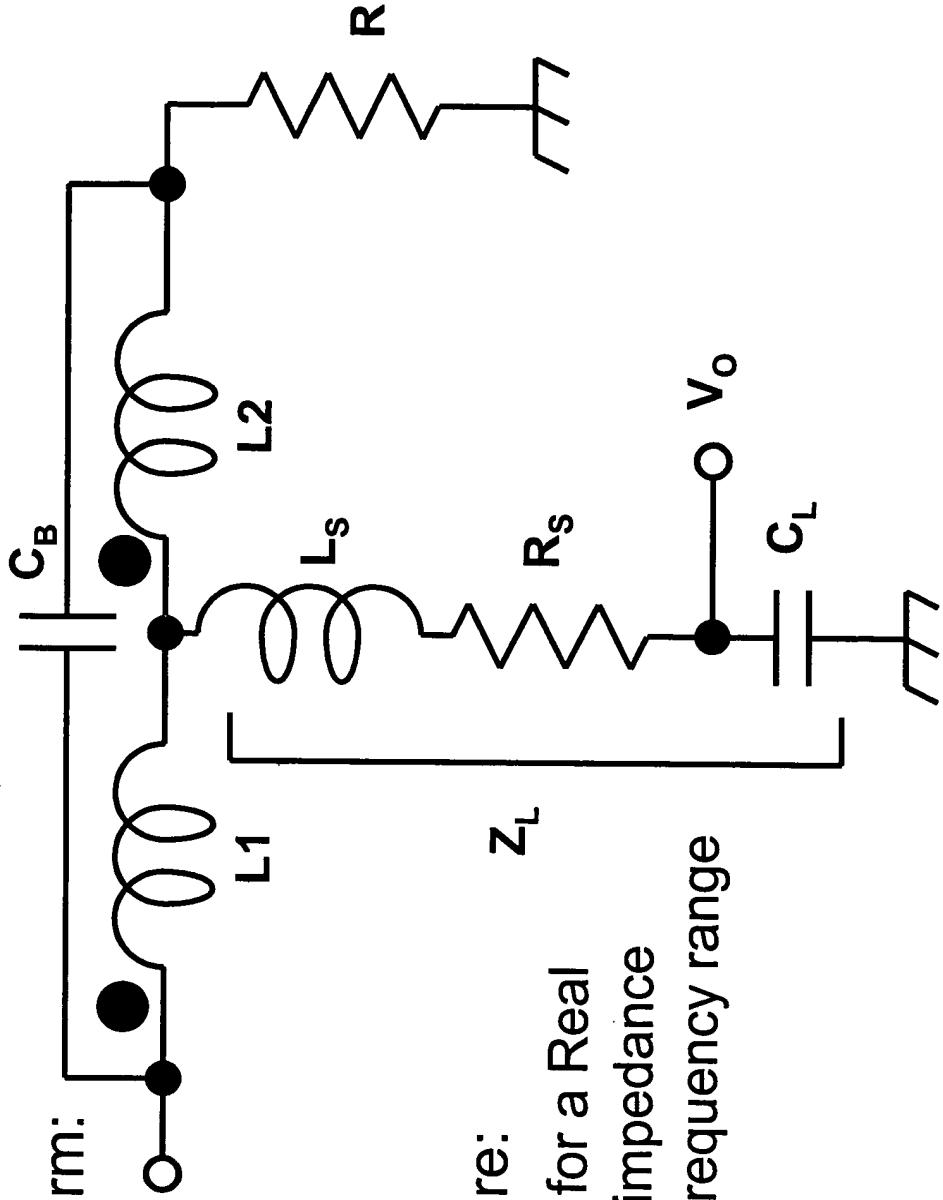


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1

What is a Bridged T-Coil?

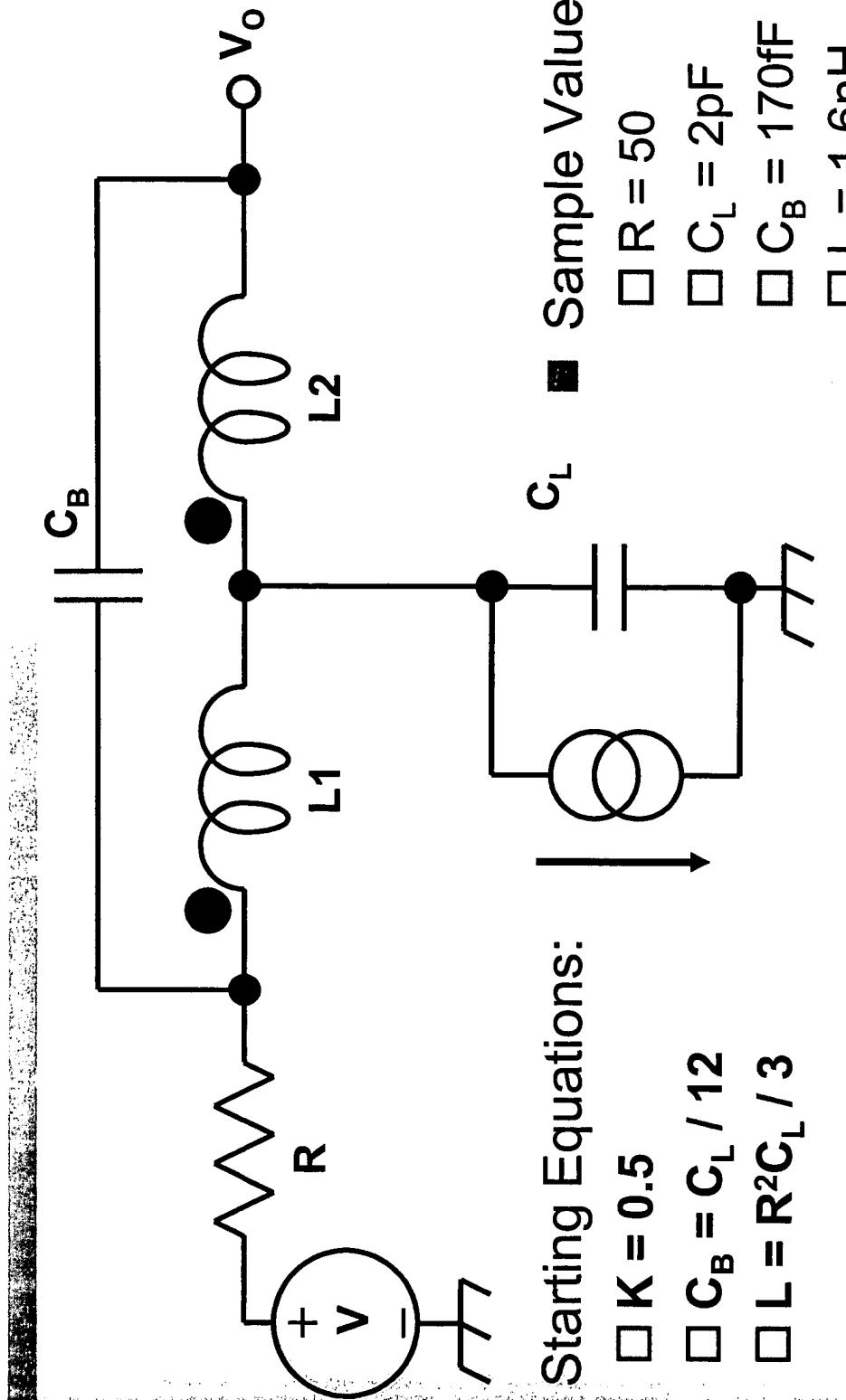
The General Form:



Important Feature:

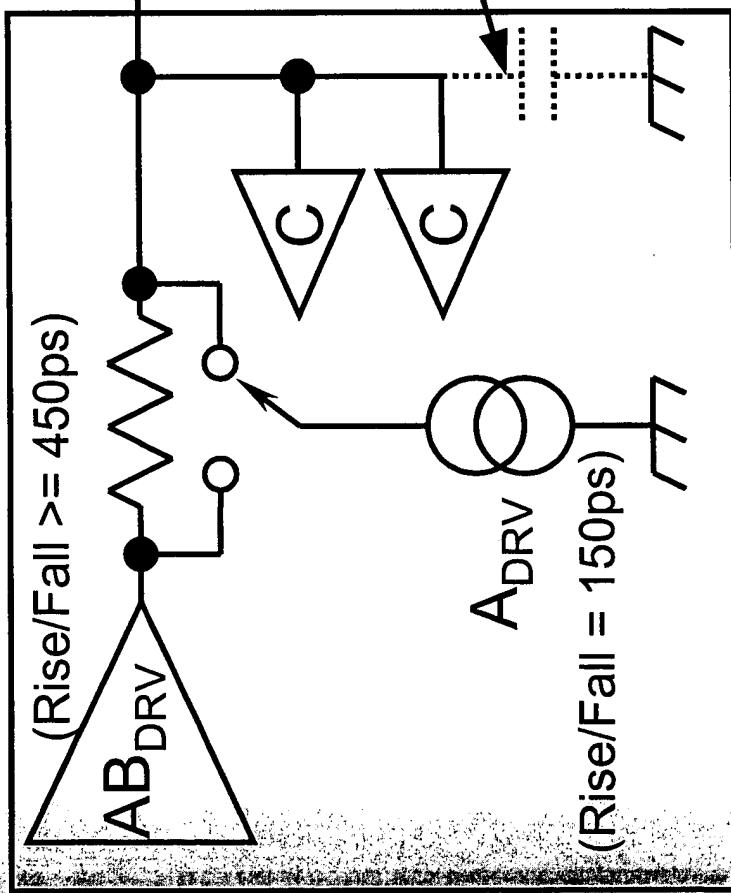
- ❑ Can be tuned for a Real 50-ohm input impedance over a broad frequency range

Simplified Balanced Bridged T-Coil

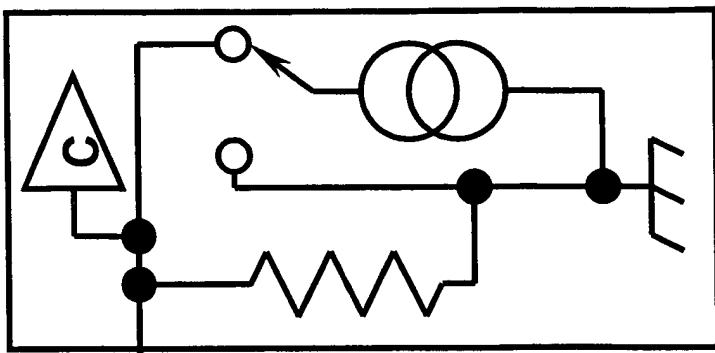


What problem are we trying to solve?

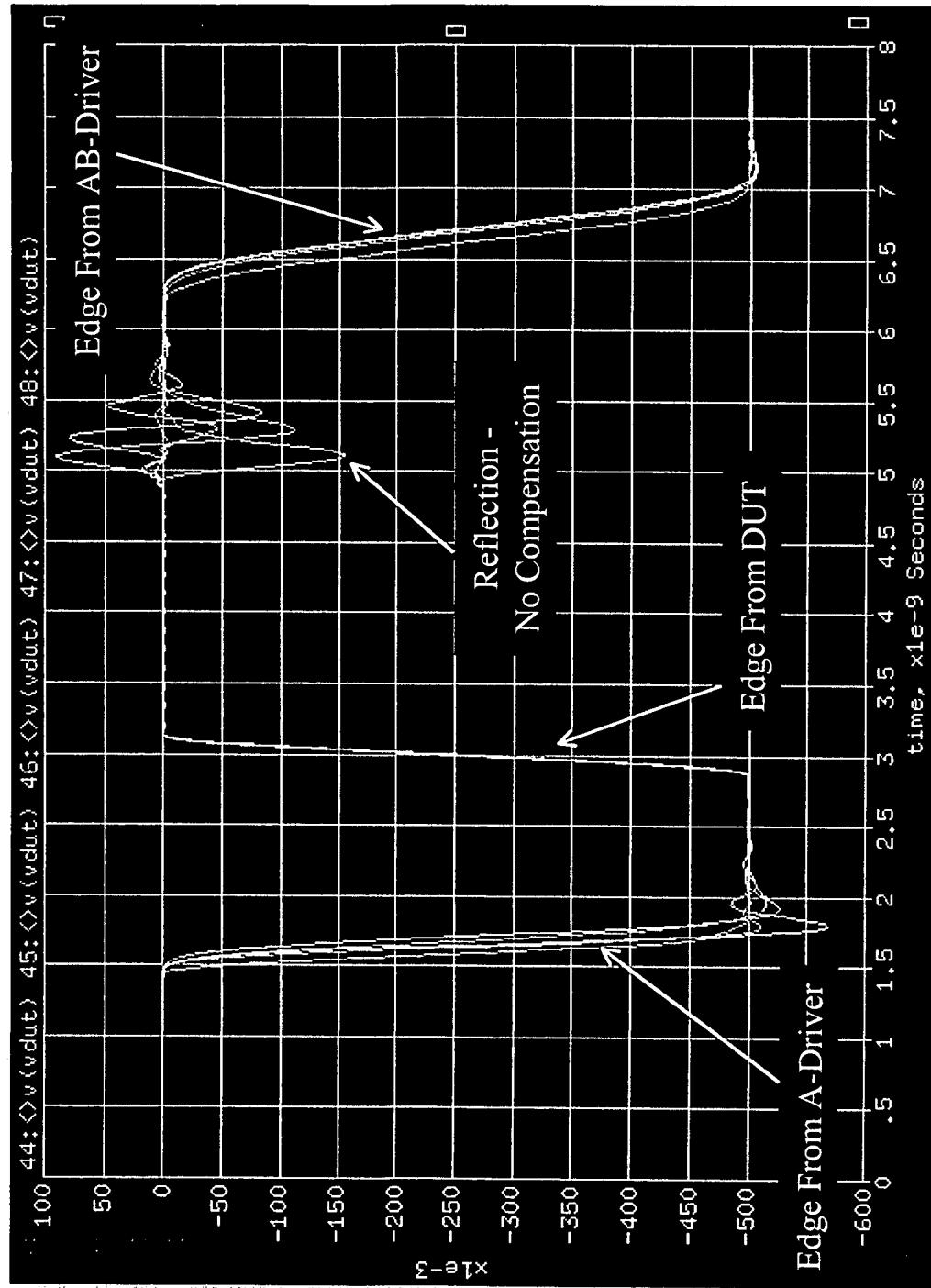
■ ATE Tester Pin Channel



■ DUT

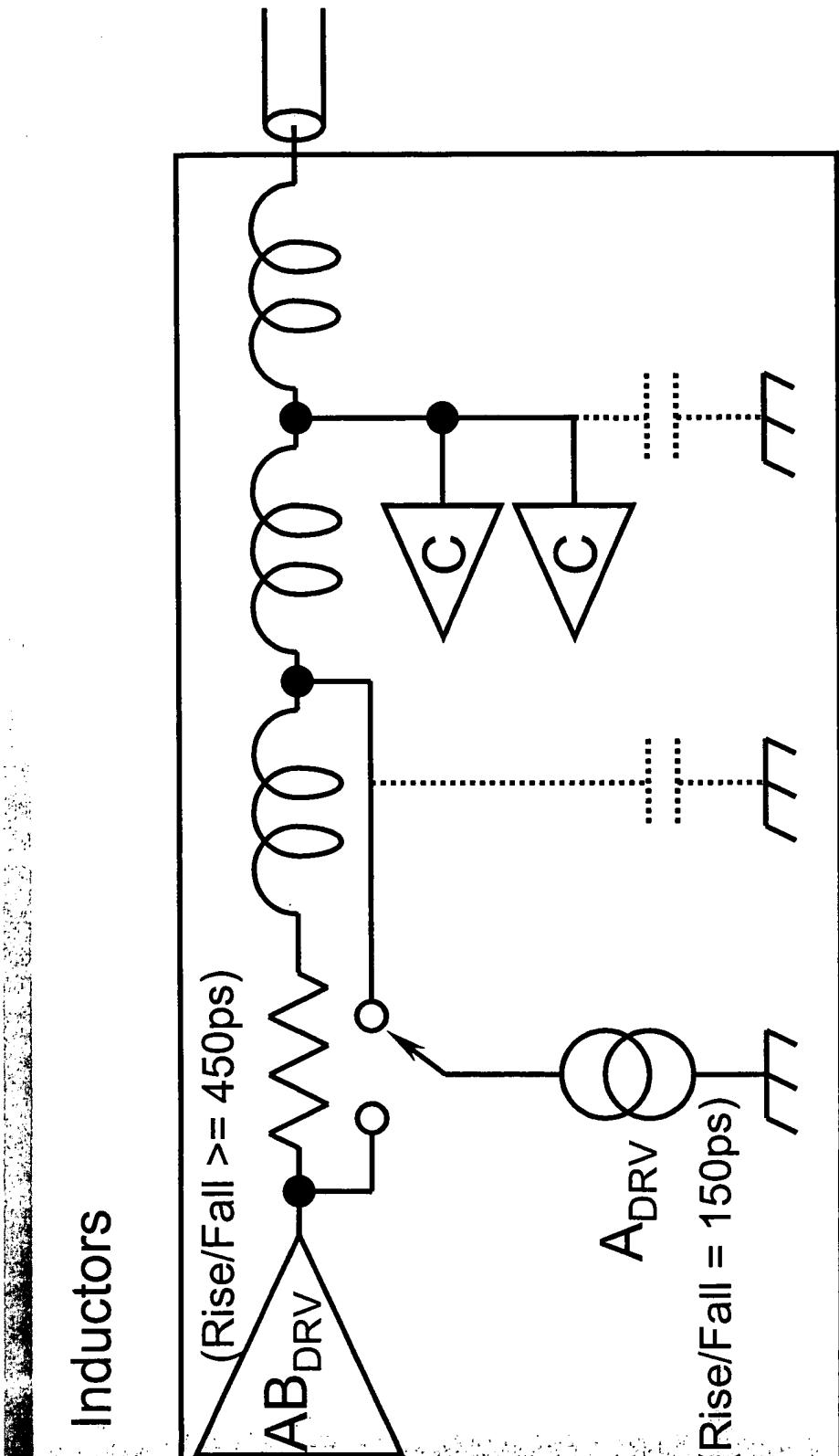


An Example Waveform (DUT End)



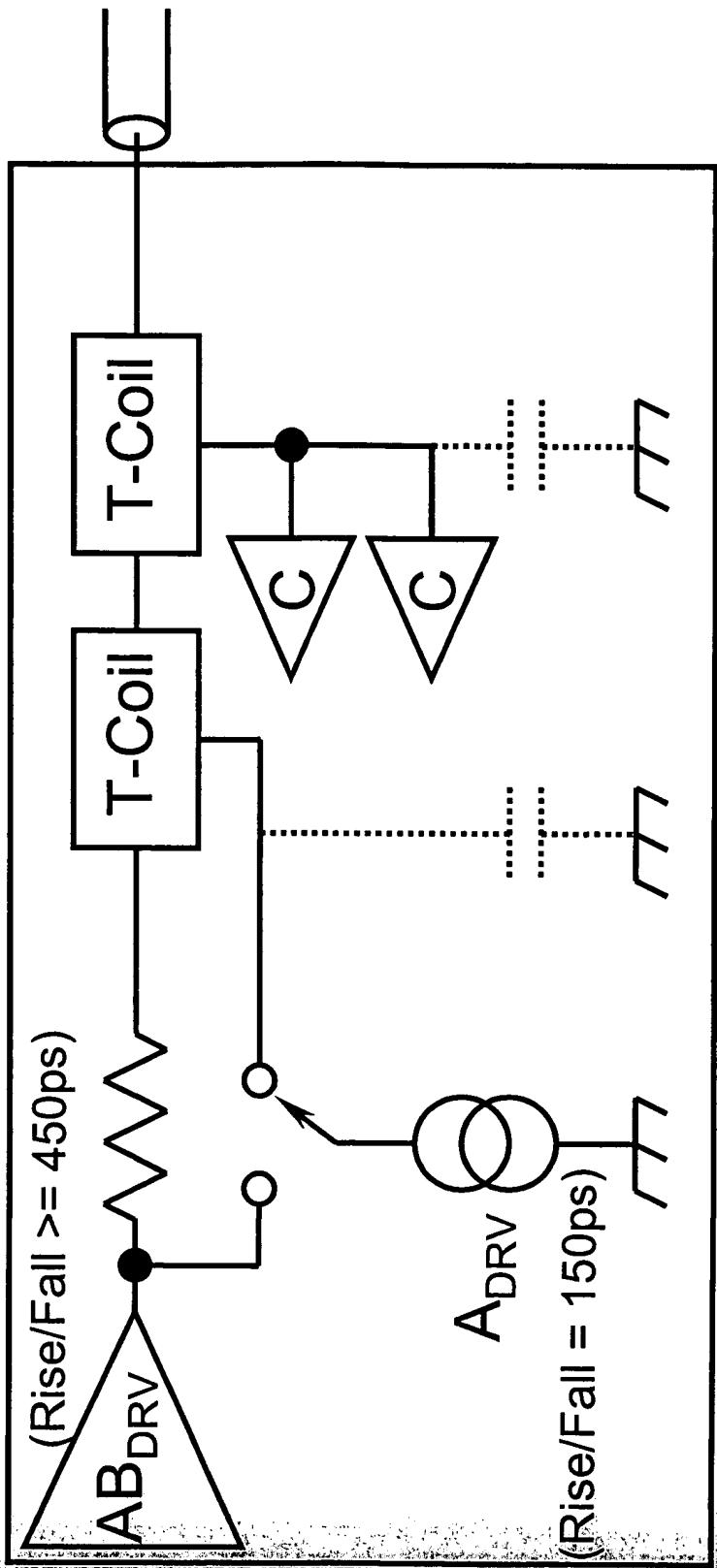
How Do We Compensate?

■ Inductors



How Do We Compensate?

T-Coils



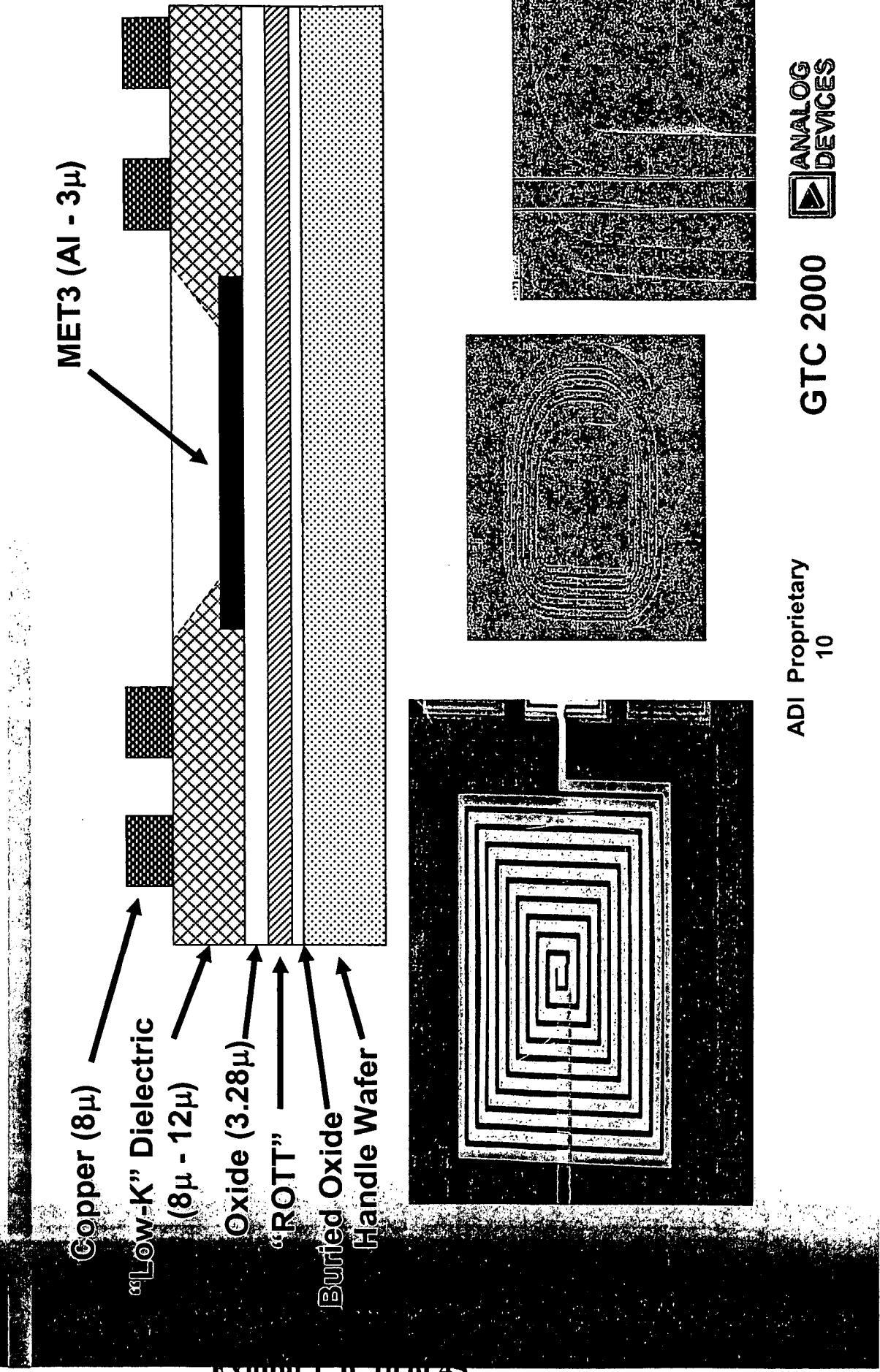
Key Inductor Performance Issues

- Low Resistance
- High "Q"
- Low Capacitance
- Small Size
- ADI Semiconductor Process Compatible

What Processes Are Available?

- MET3 Inductors On XF2 - 3 μ M Thick Aluminum
- CU Inductors, 8 μ M Thick Post-Processed on 12 μ M of Low-K Dielectric (K=2.7) (MEMSCAP)
- CU Inductors, 8 μ M Thick Post-Processed on 8 μ M of Low-K Dielectric (K=2.7) (Advanced MicroSensors)
- Other: Chip-On-Chip, Bond Wires, etc.

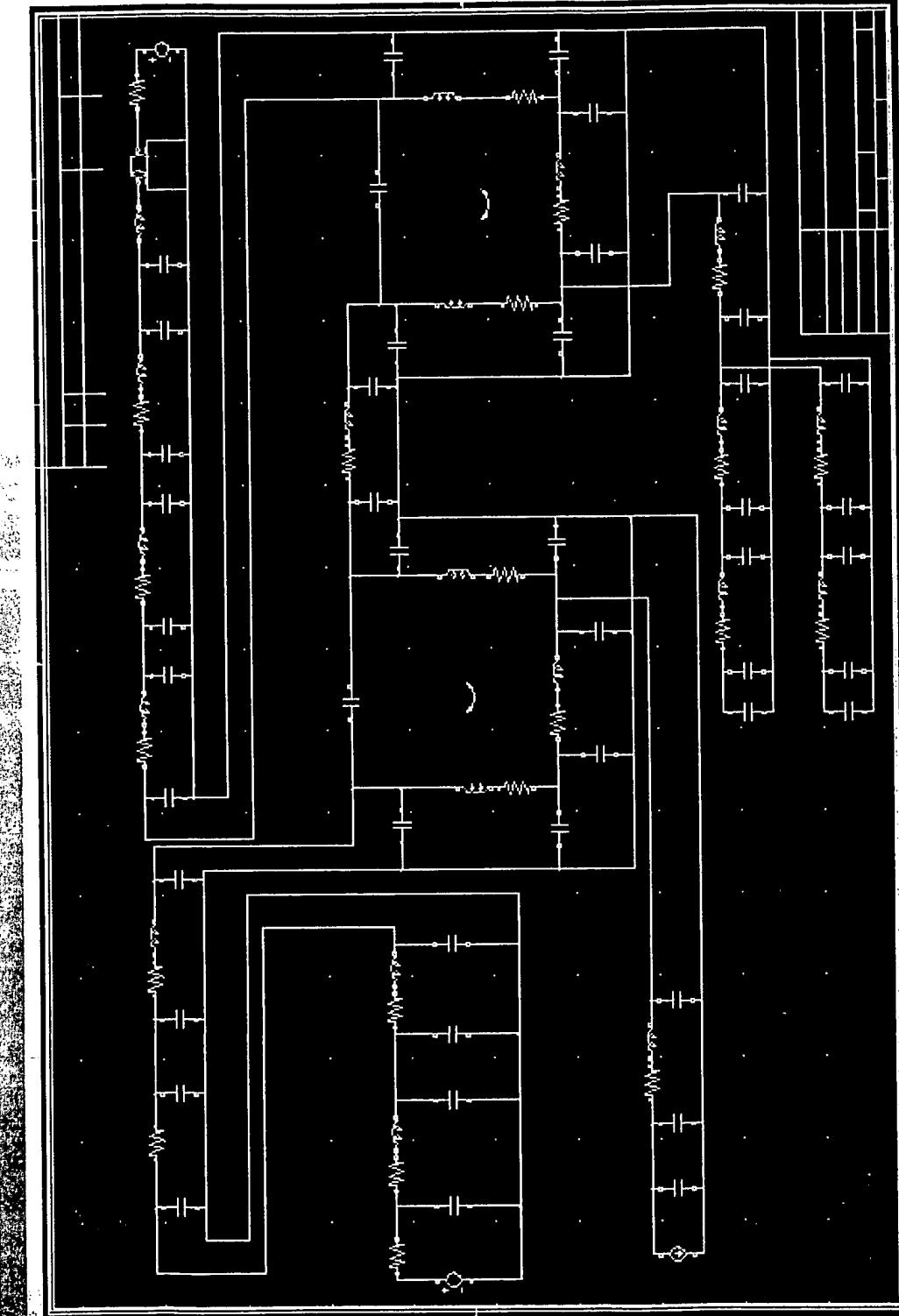
What Do The Post-Processed Structures Look Like?



How Well Do T-Coils Work?

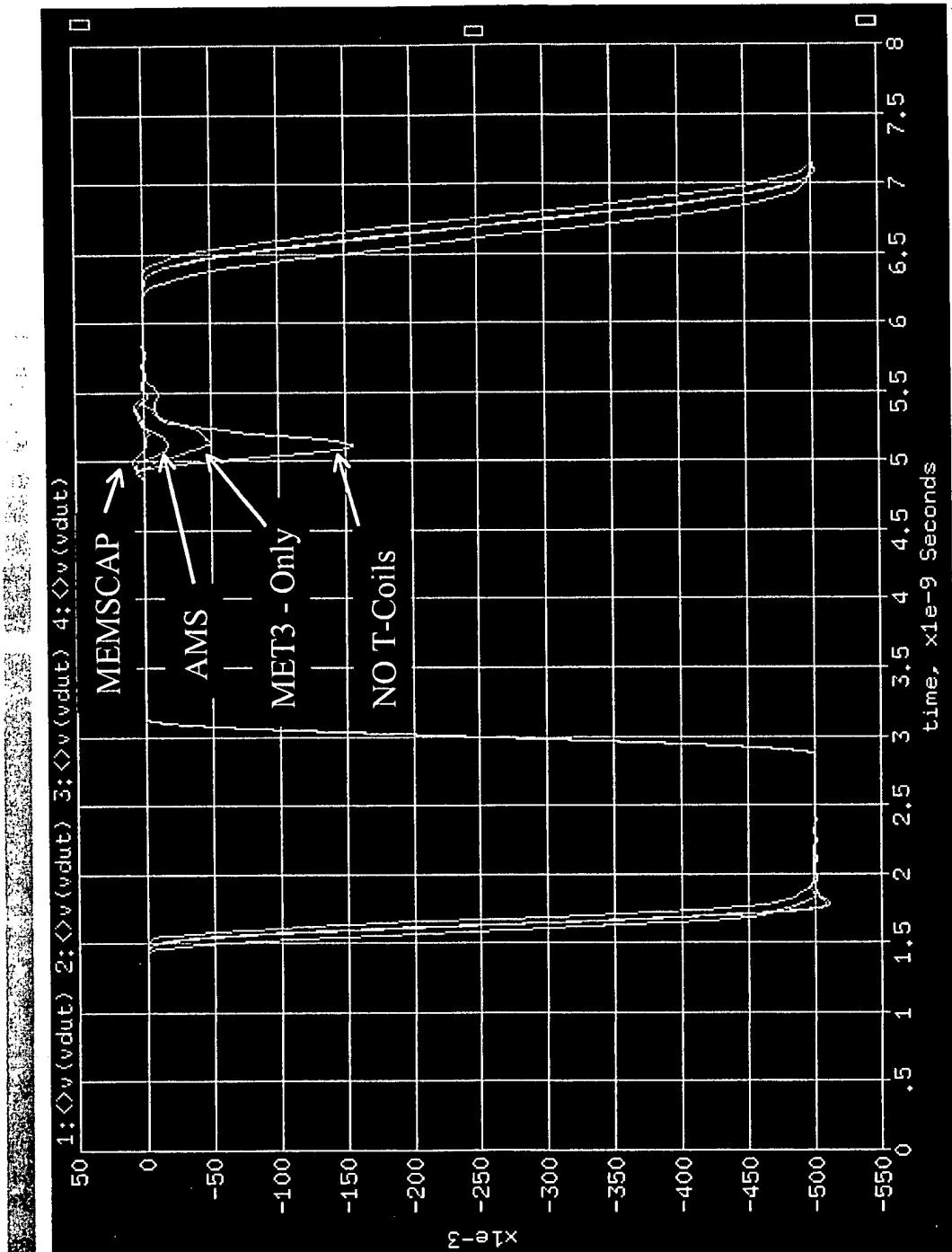
- Process Comparison: None, MET3, AMS, MEMSCAP
- Comparison to None, 1, 2 and 3-Inductor Compensation
- Single Vs. Dual T-Coils
- Sensitivity to:
 - Inductance Value
 - Comparator Capacitance
 - Class-A Driver Capacitance
 - Metal Parasitic Capacitance
 - Inductor Coupling Coefficient
 - Bridge Capacitor Value
 - Trace and Coil Series Resistance

Simulation Schematic



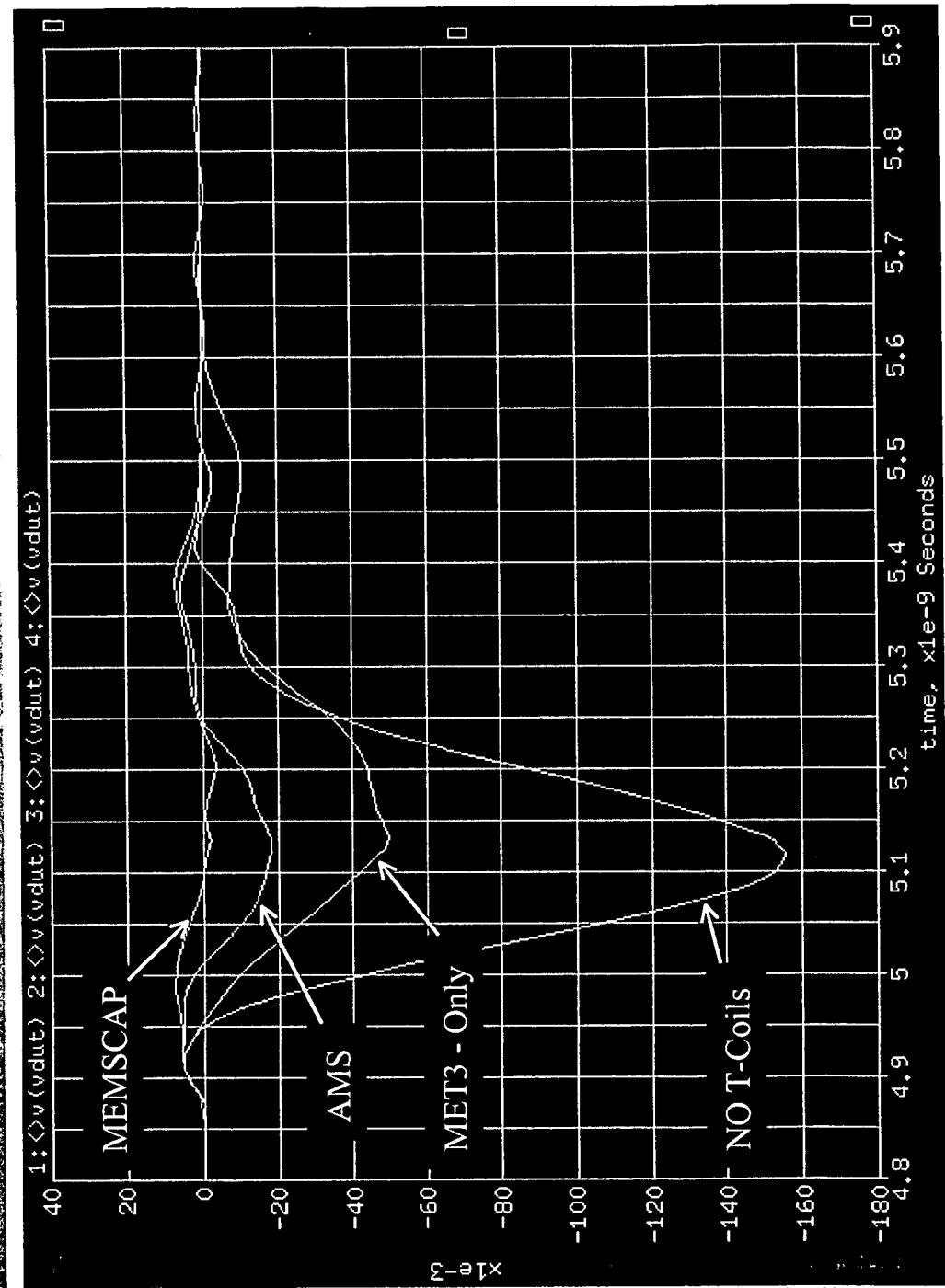
T-Coils Compared by Processes

Composite Overview Waveform at DUT



T-Coils Compared by Process

Composite Overview Waveform at DUT - Reflection

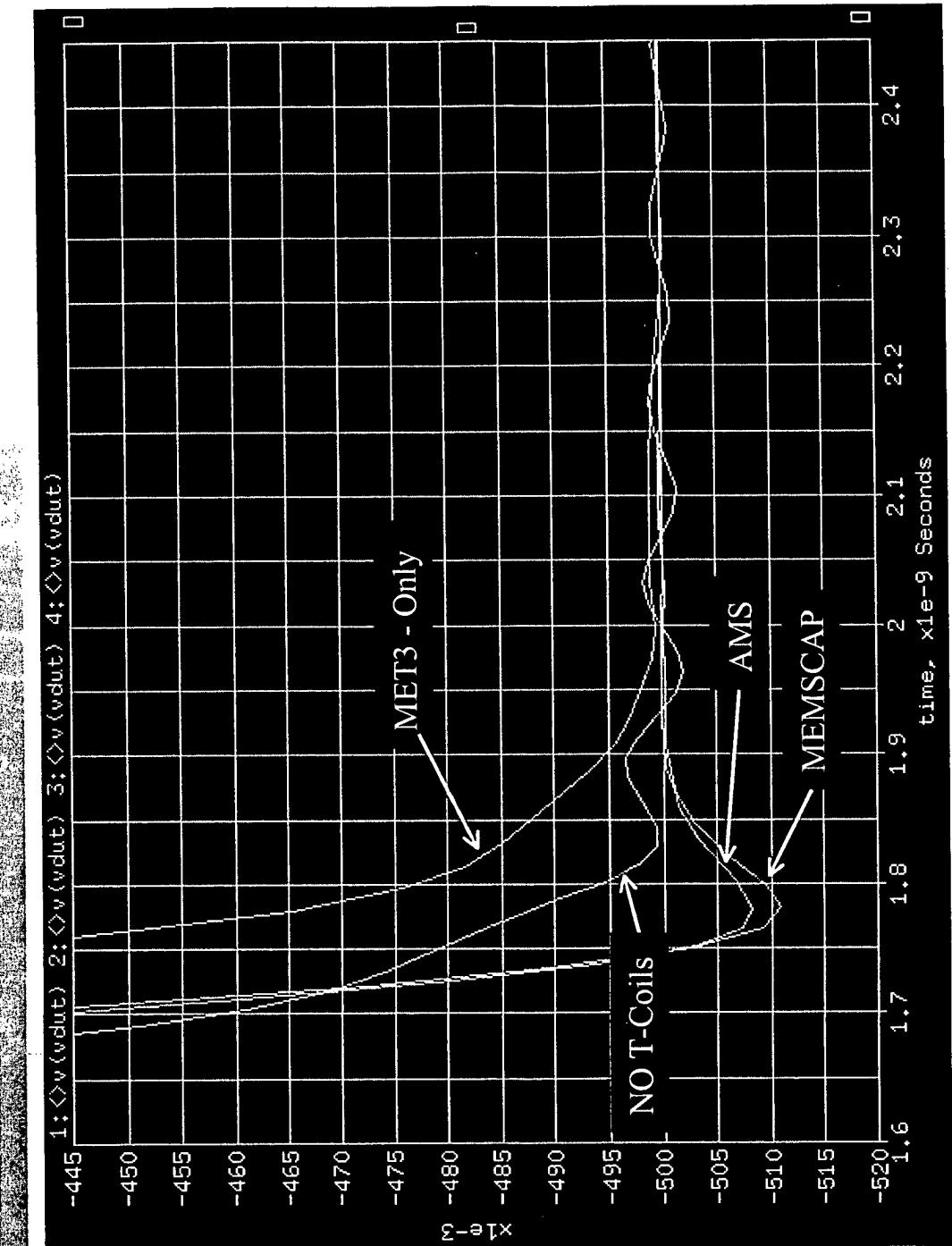


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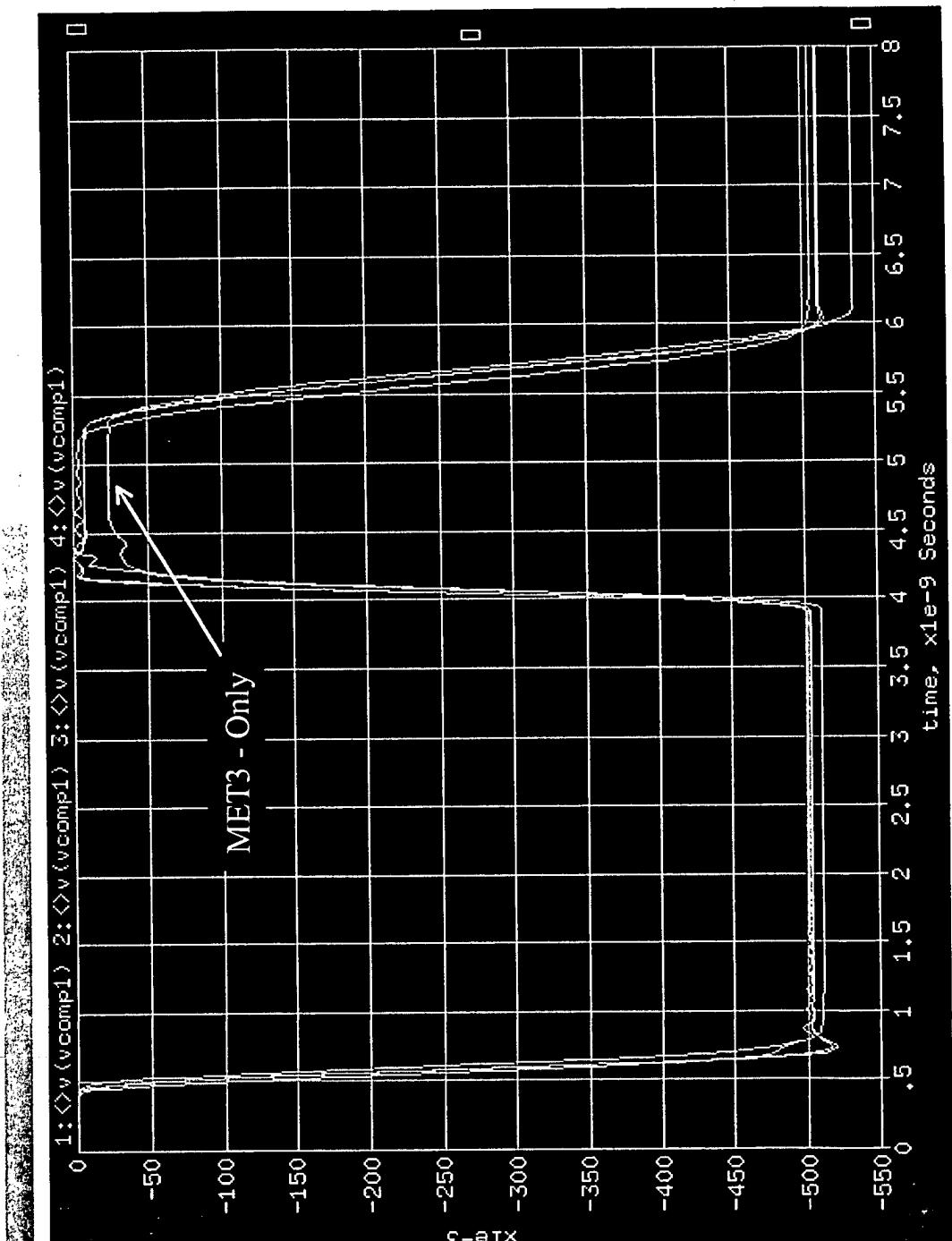
T-Coils Compared by Process

Composite Overview Waveform at DUT - Incident Edge



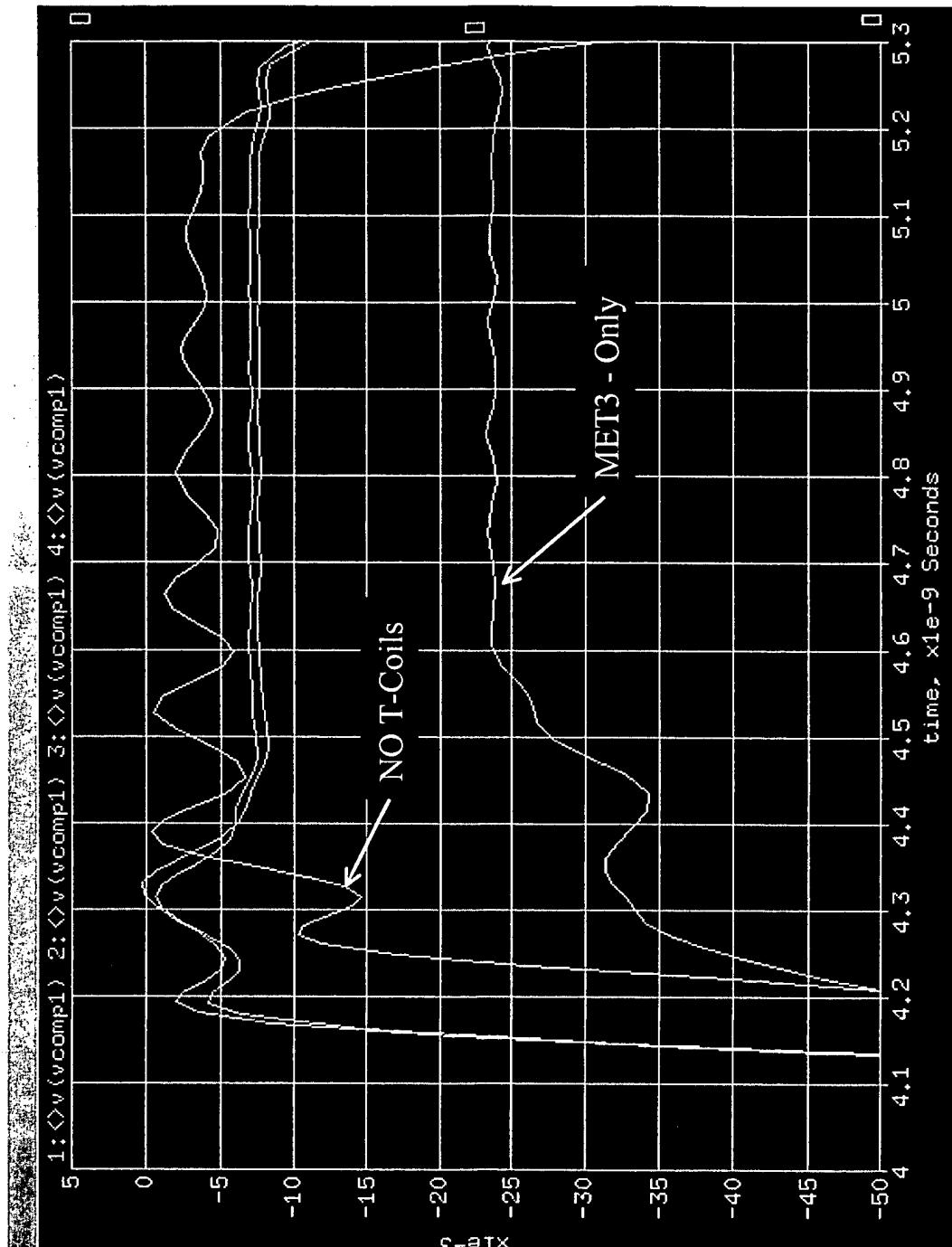
T-Coils Compared by Process

Composite Overview Waveform at Comparator



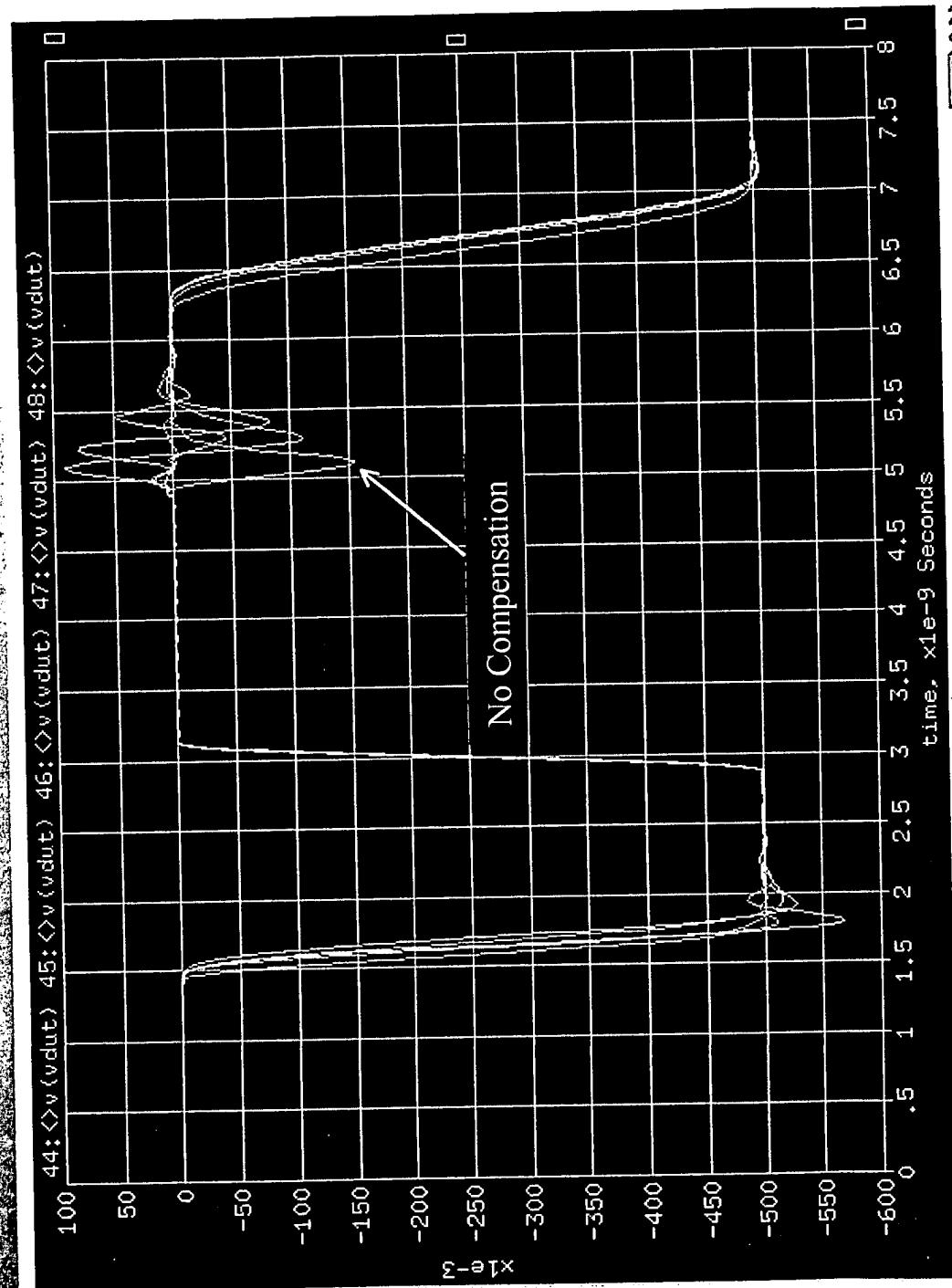
T-Coils Compared by Process

Composite Overview Waveform at Comparator Enlarged



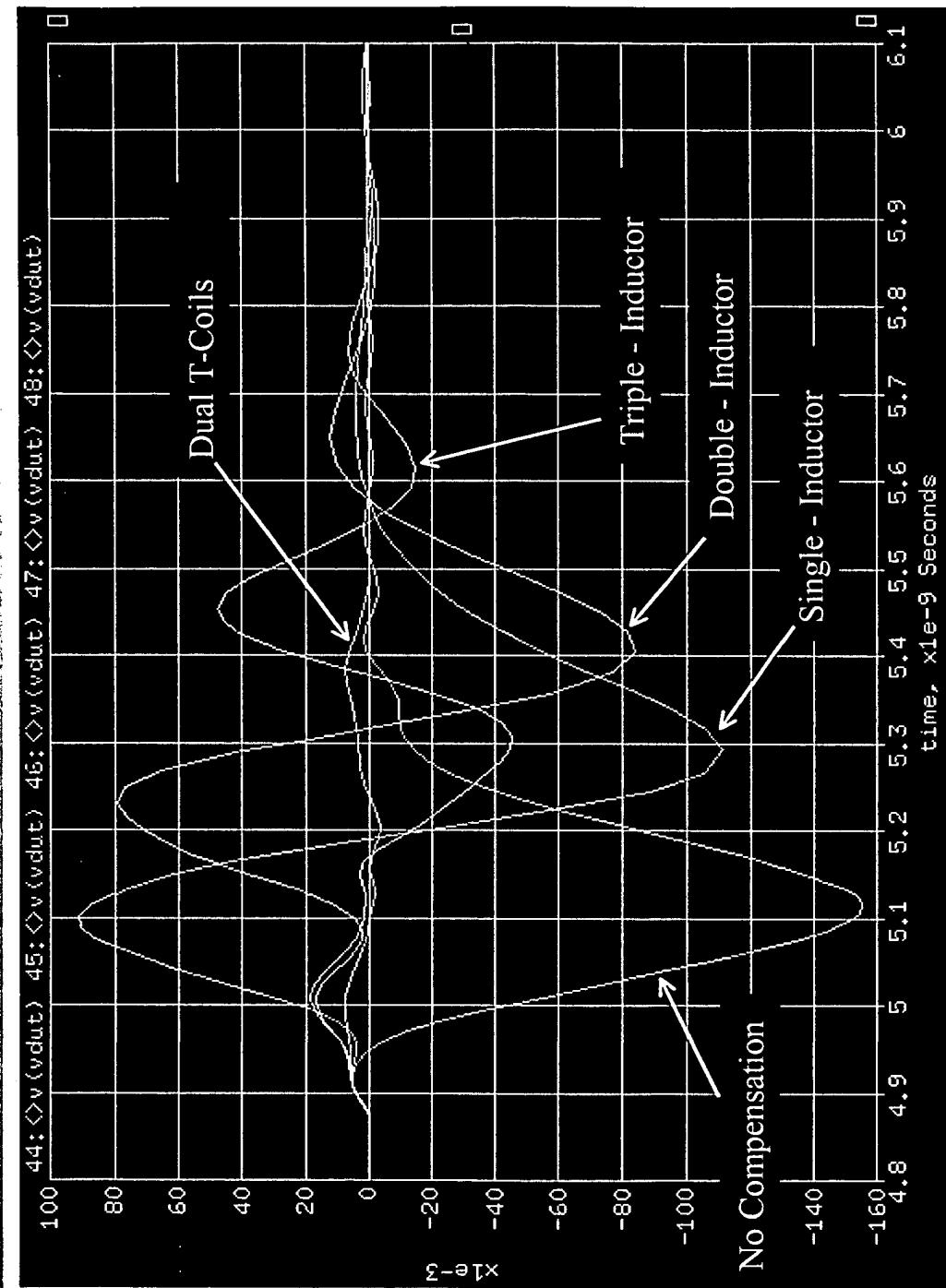
T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at DUT



T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at DUT - Reflection

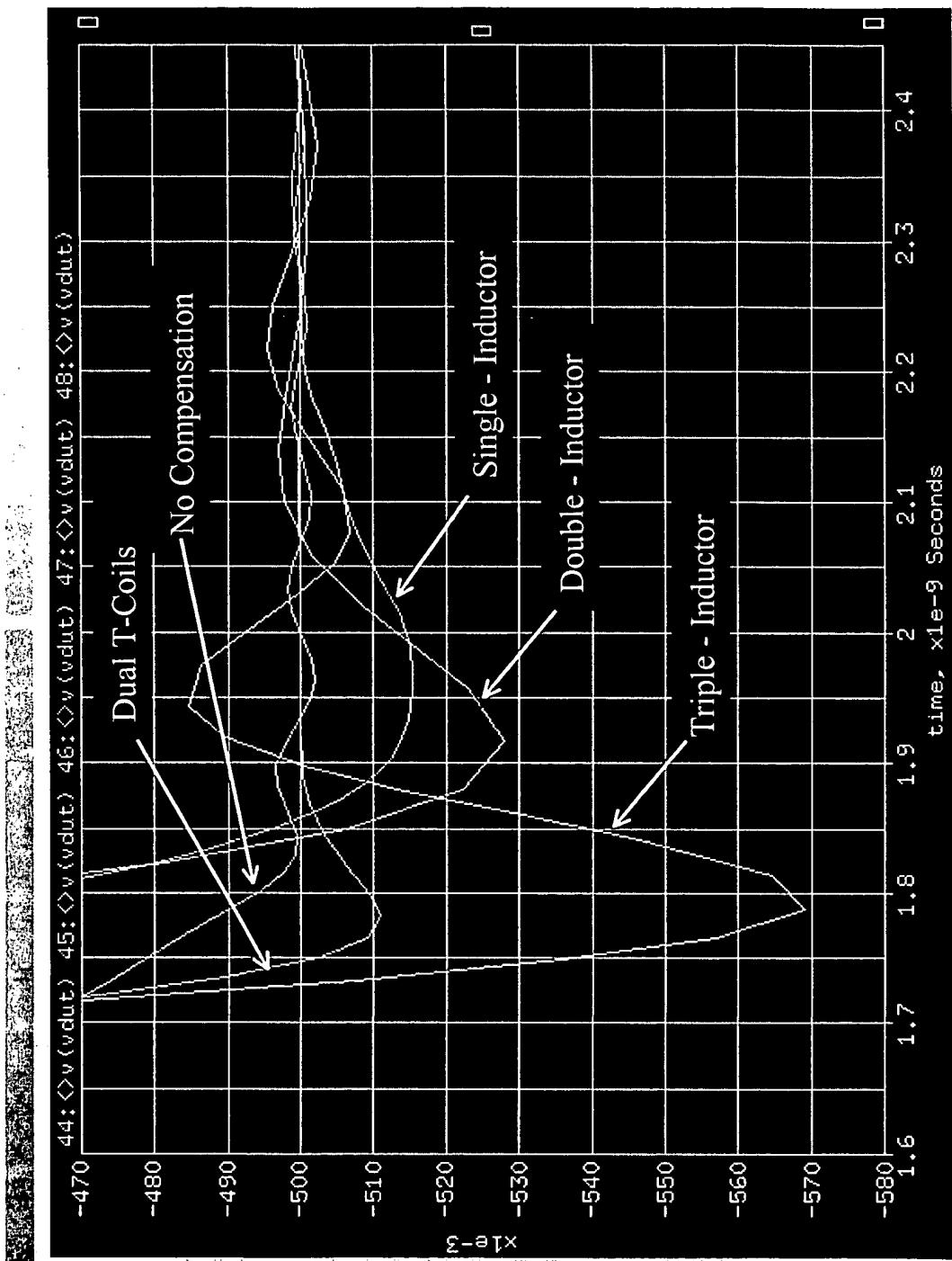


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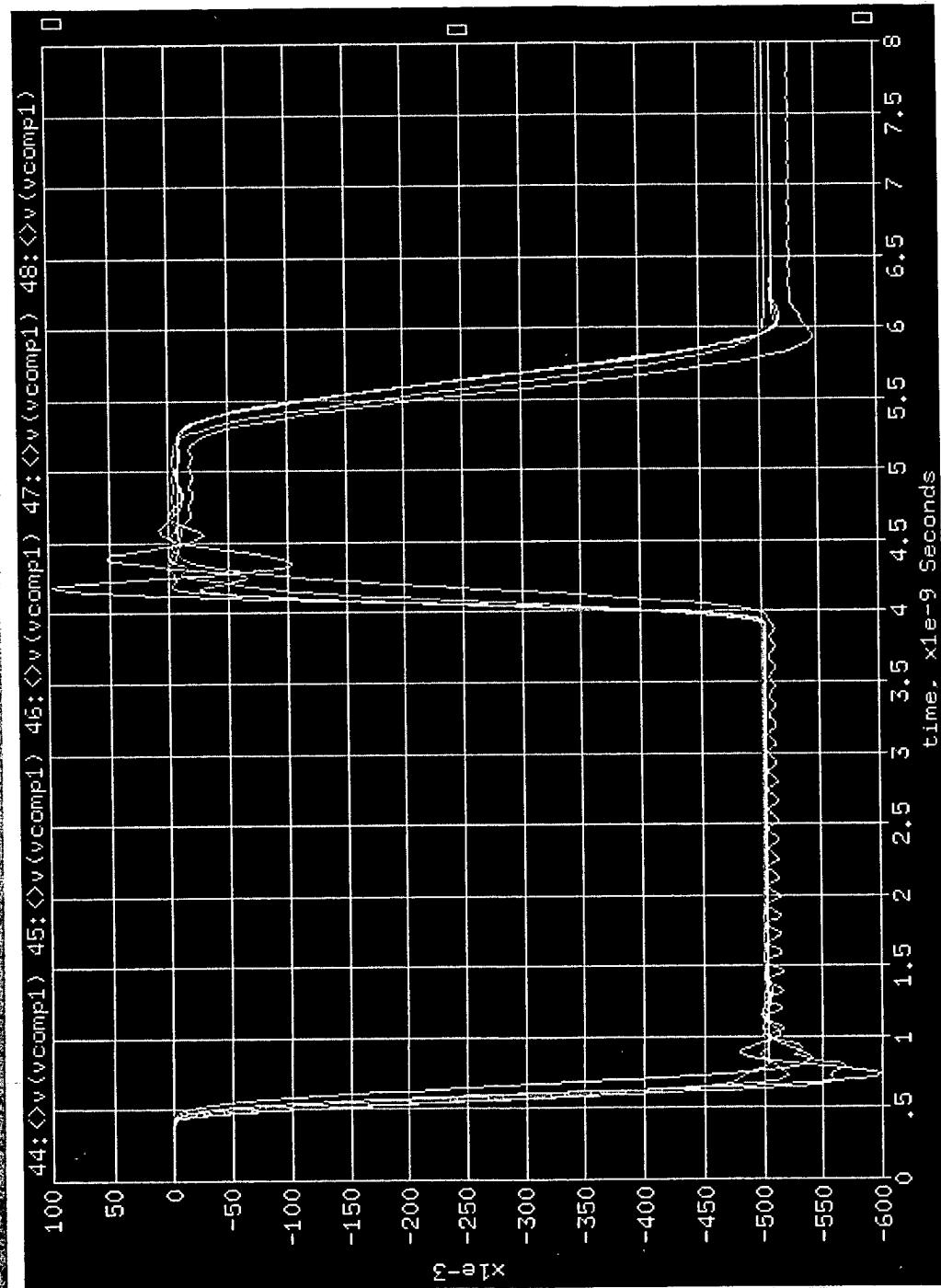
T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at DUT - Incident Edge



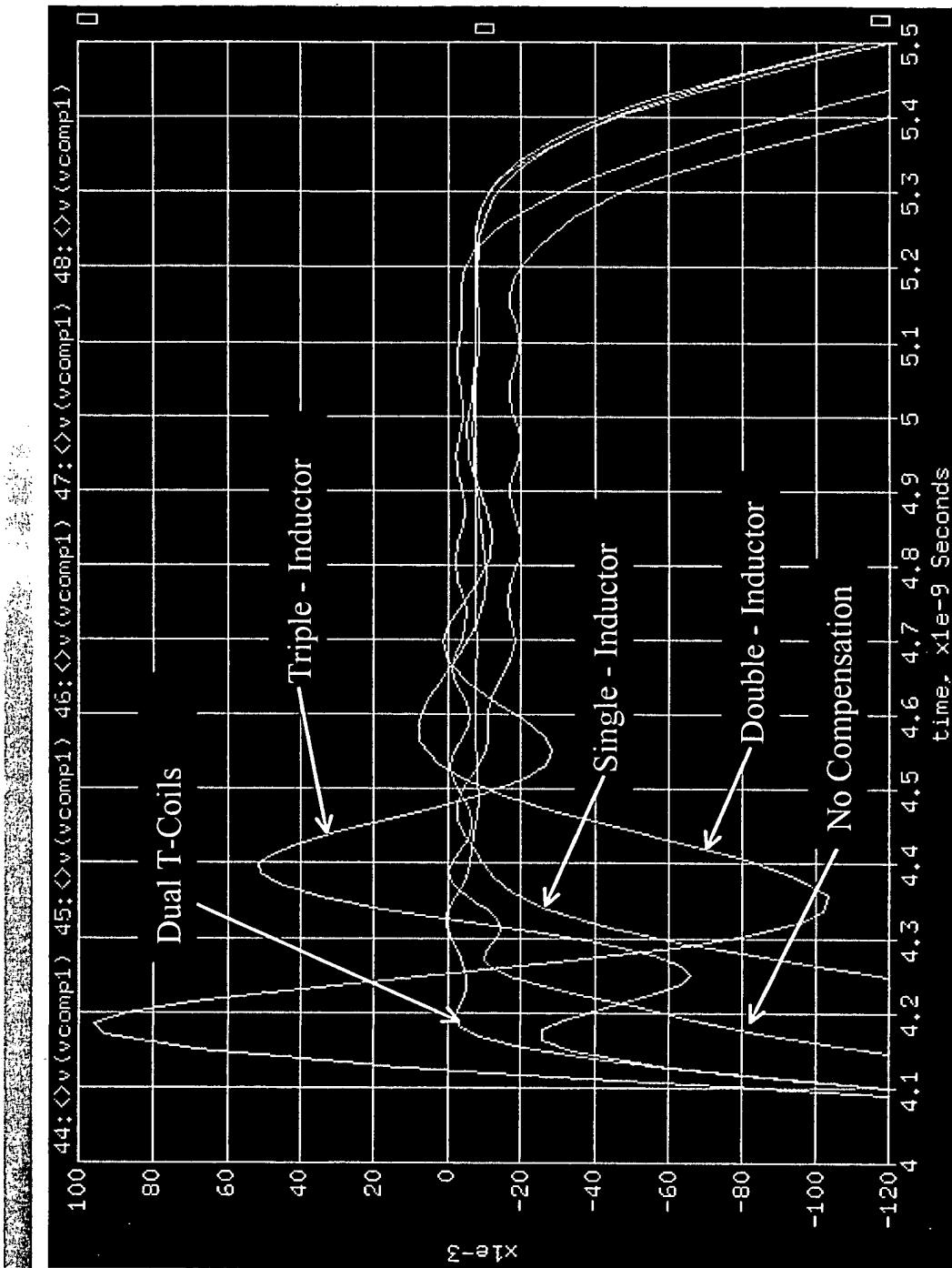
T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at Comparator



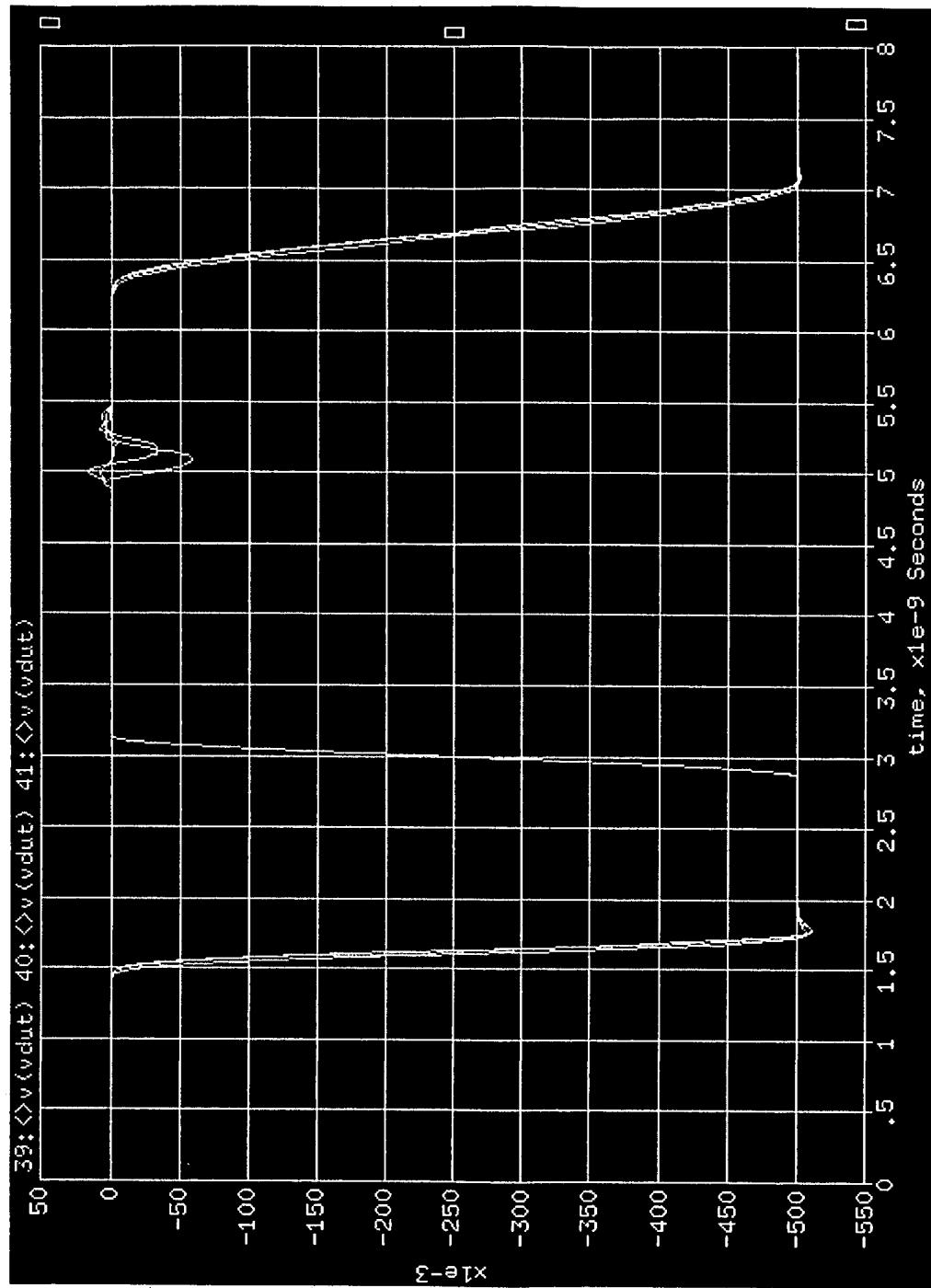
T-Coils Compared To 0, 1, 2, 3 Inductors

Composite Overview Waveform at Comparator Enlarged



One Vs. Two T-Coils Compared

■ Composite Overview Waveform at DUT



One Vs. Two T-Coils Compared

Composite Overview Waveform at DUT - Reflection

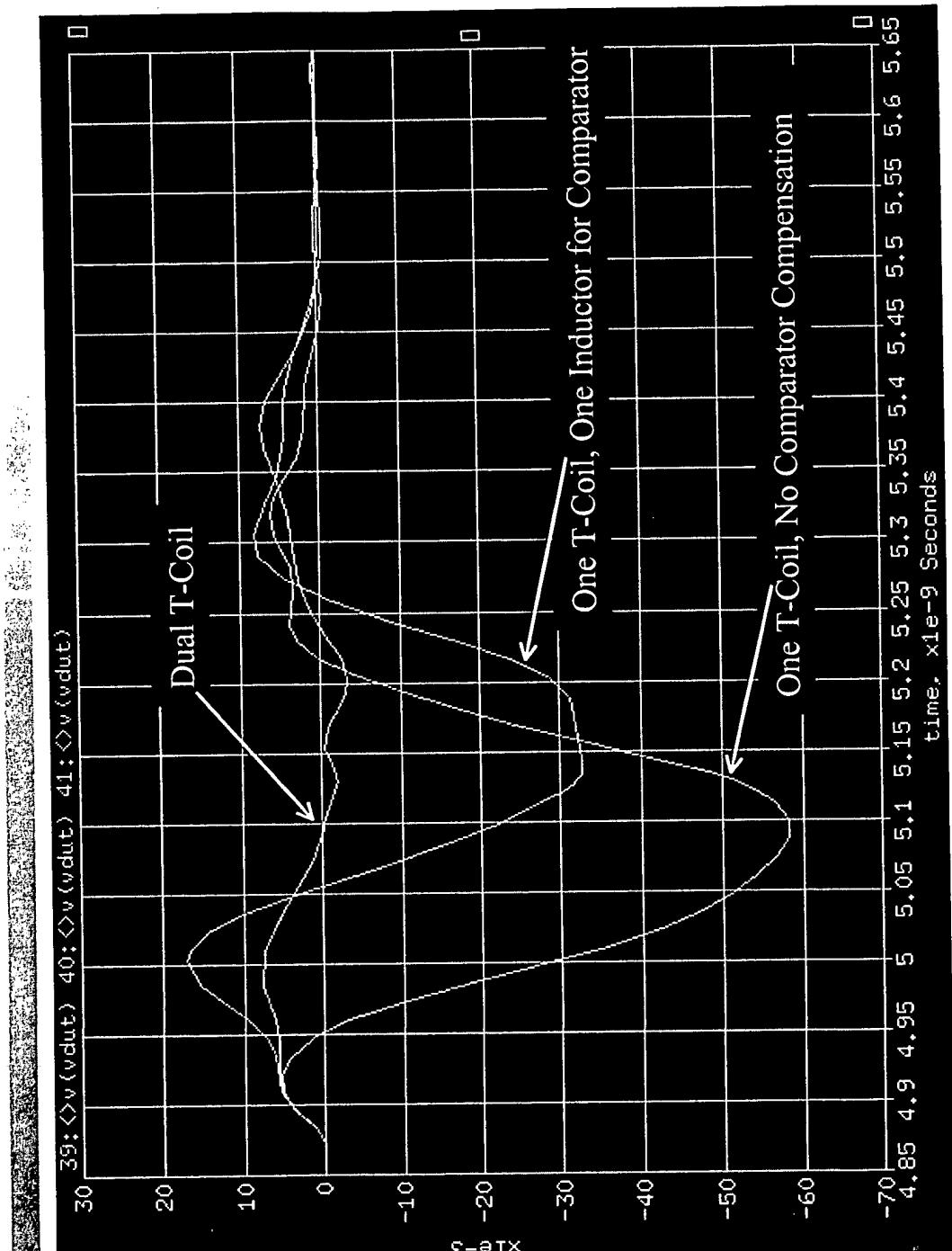
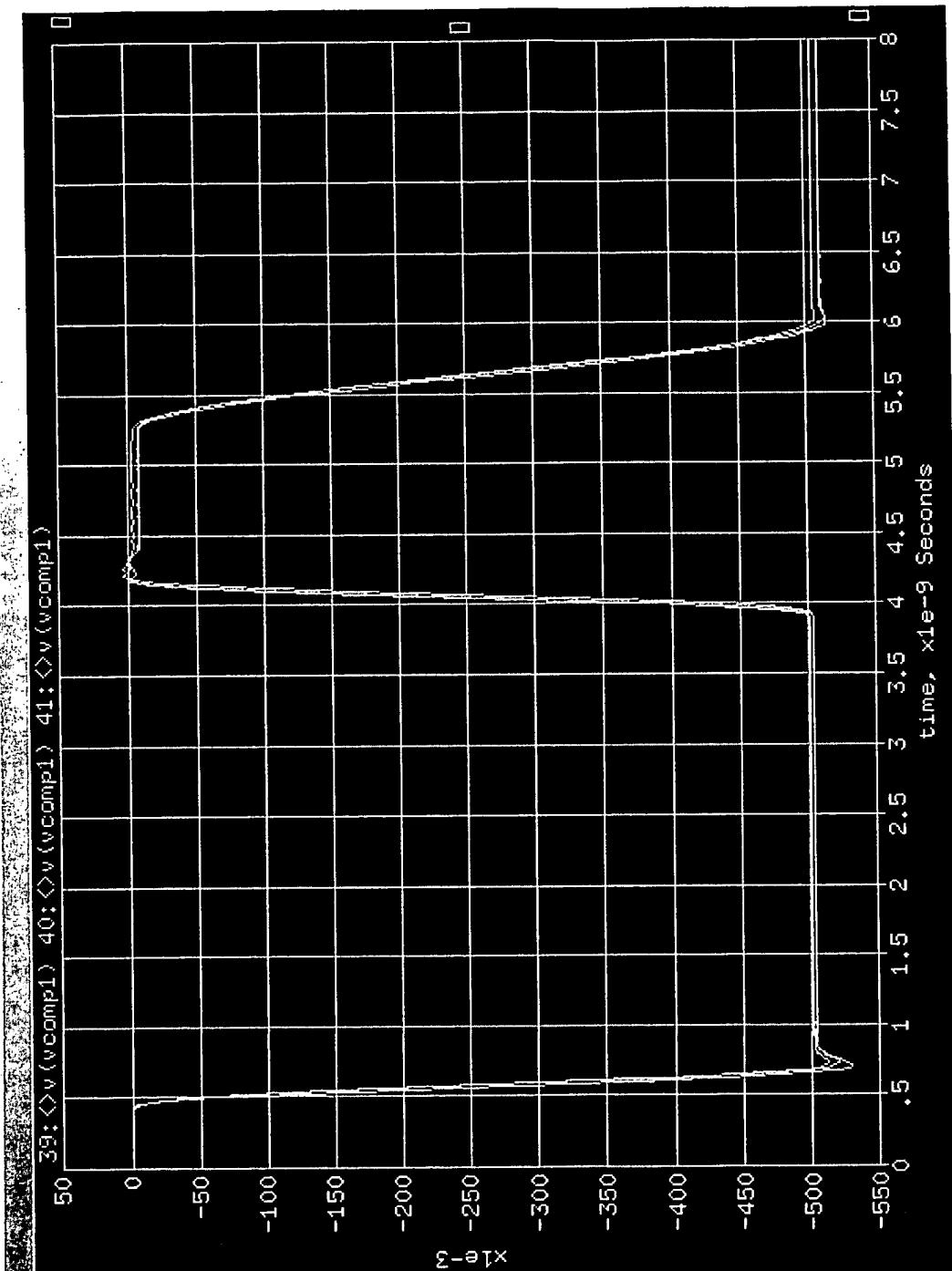


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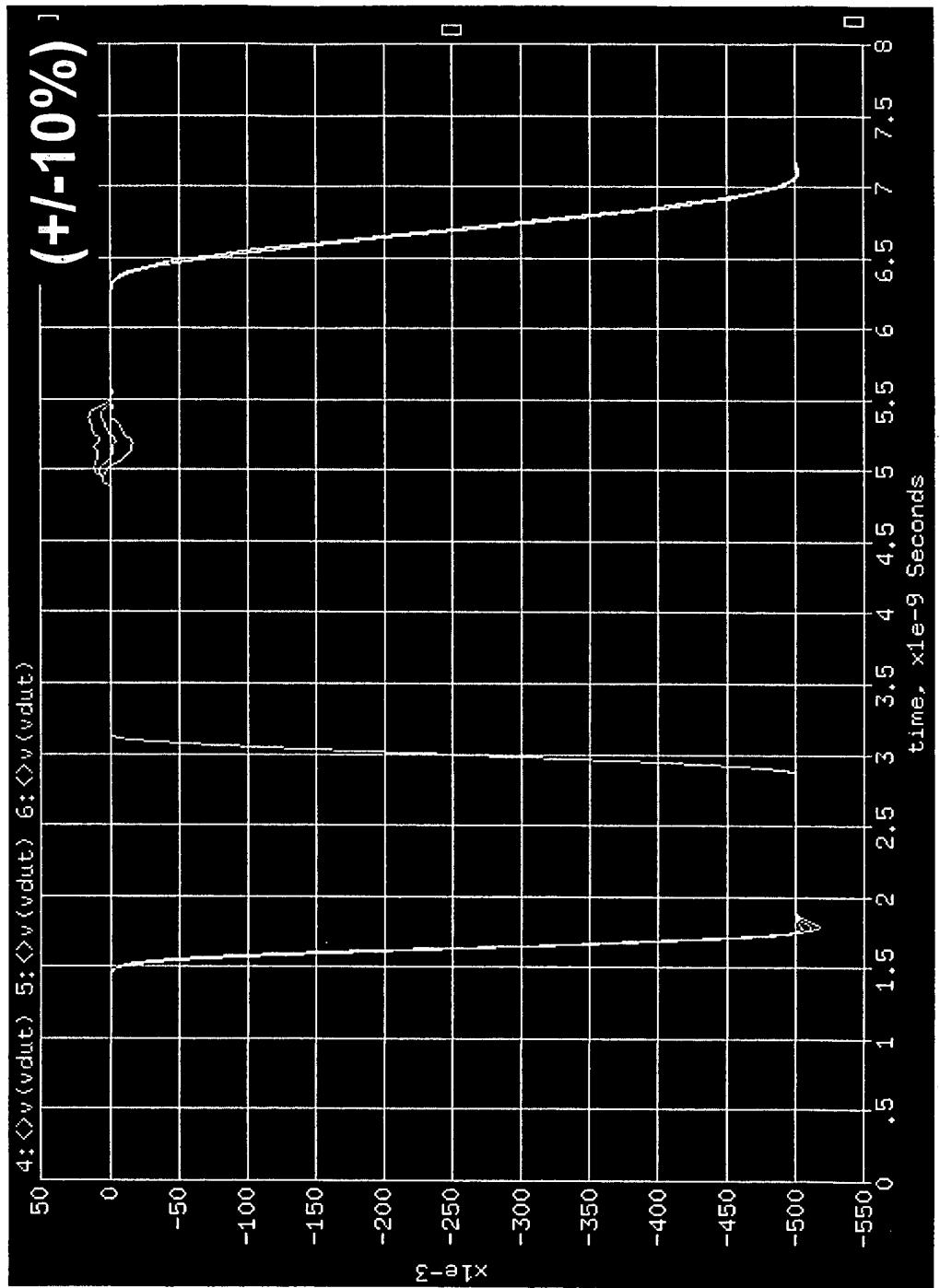
One vs. Two T-Coils Compared

Composite Overview Waveform at Comparator



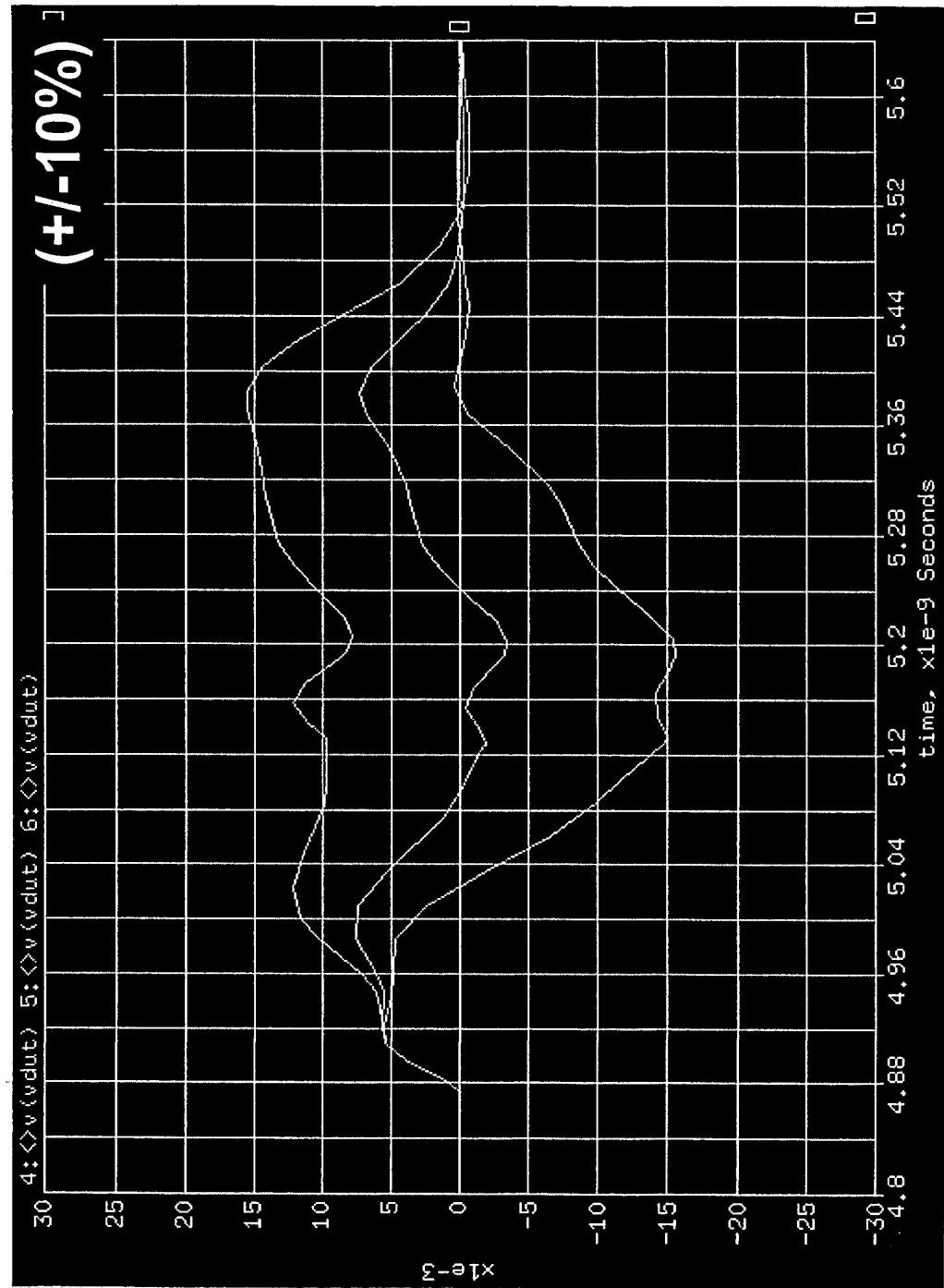
Sensitivity To Inductance Value

Composite Overview Waveform at DUT



Sensitivity To Inductance Value

Composite Overview Waveform at DUT - Reflection

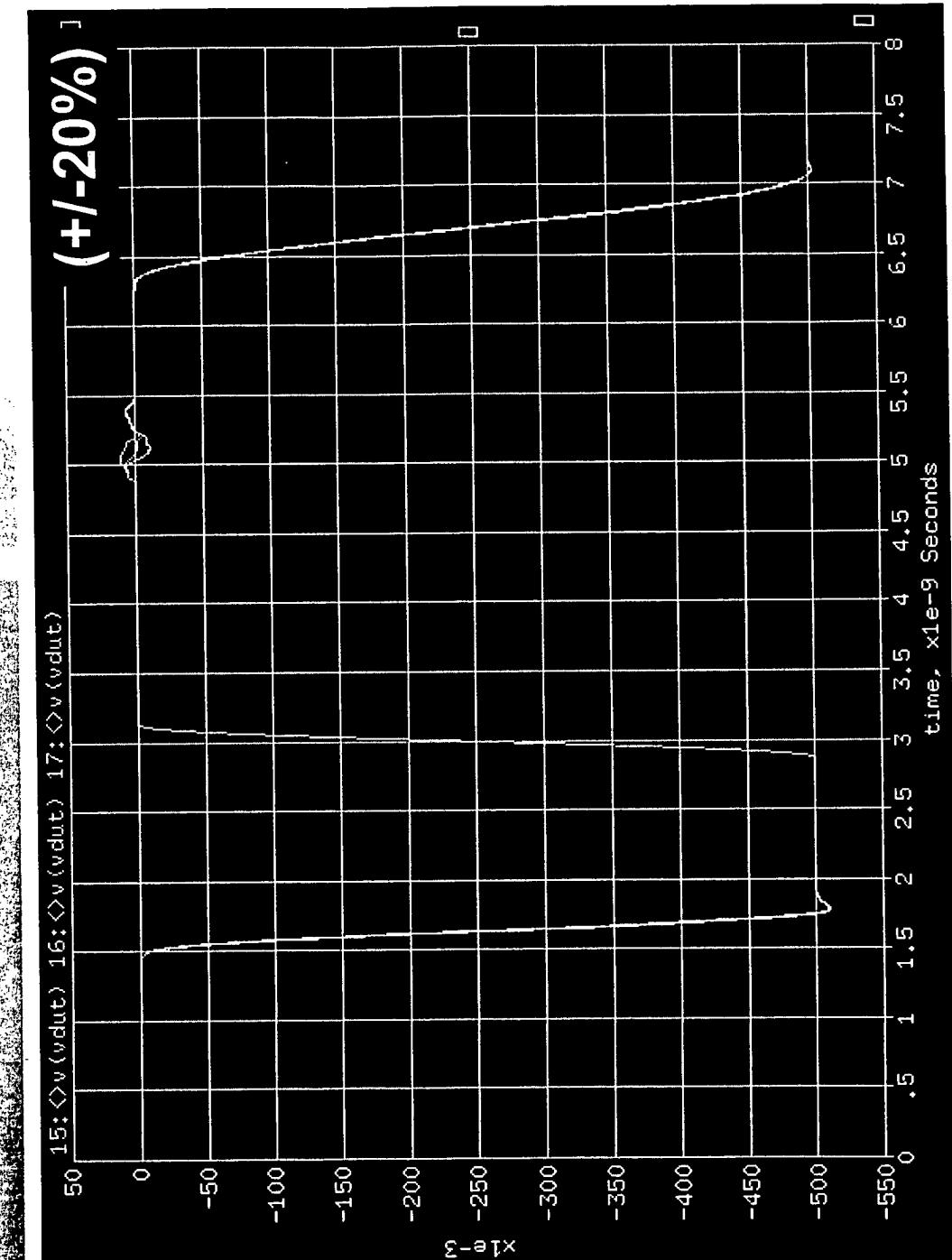


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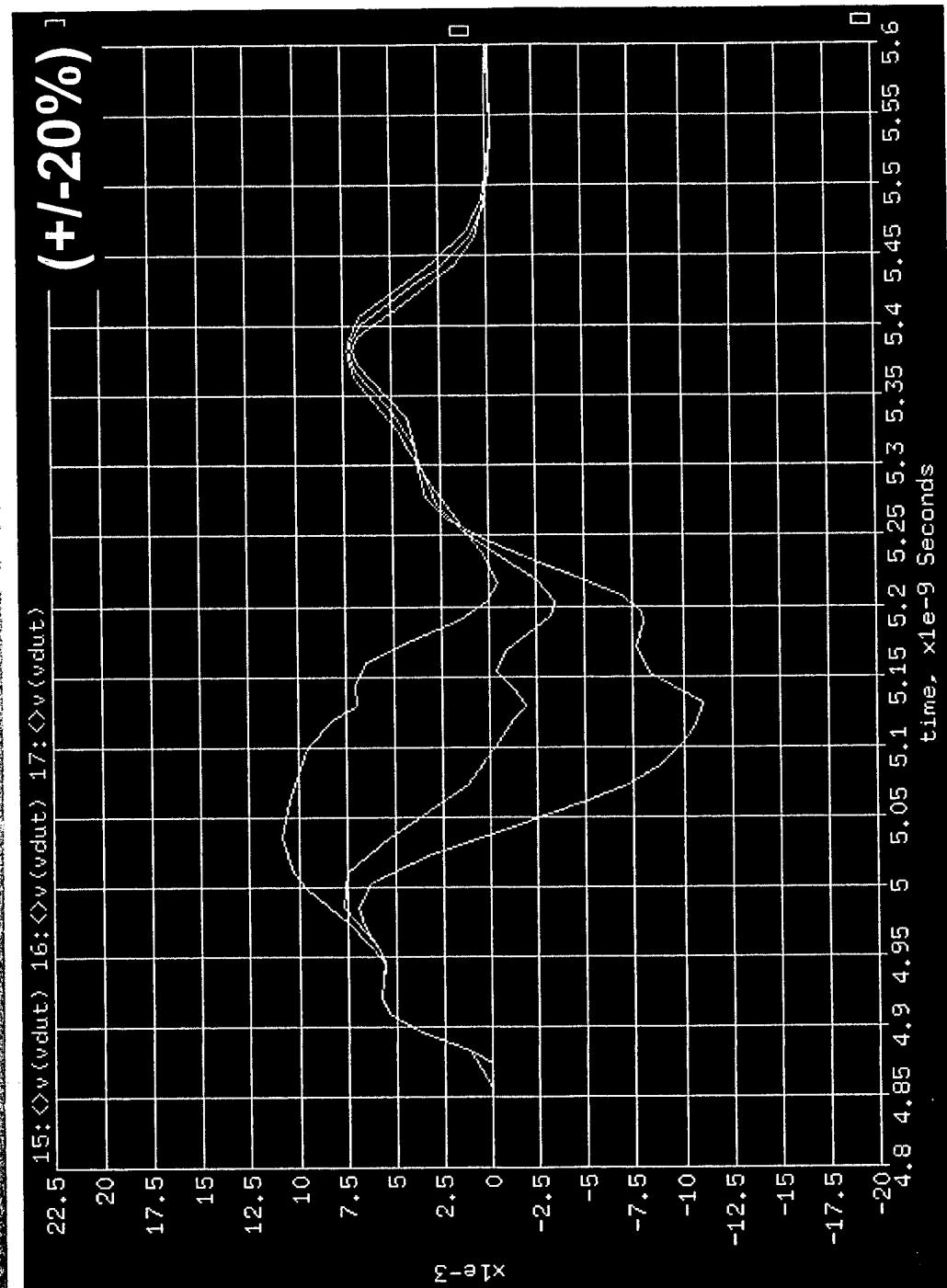
Sensitivity To Comparator Capacitance

Composite Overview Waveform at DUT



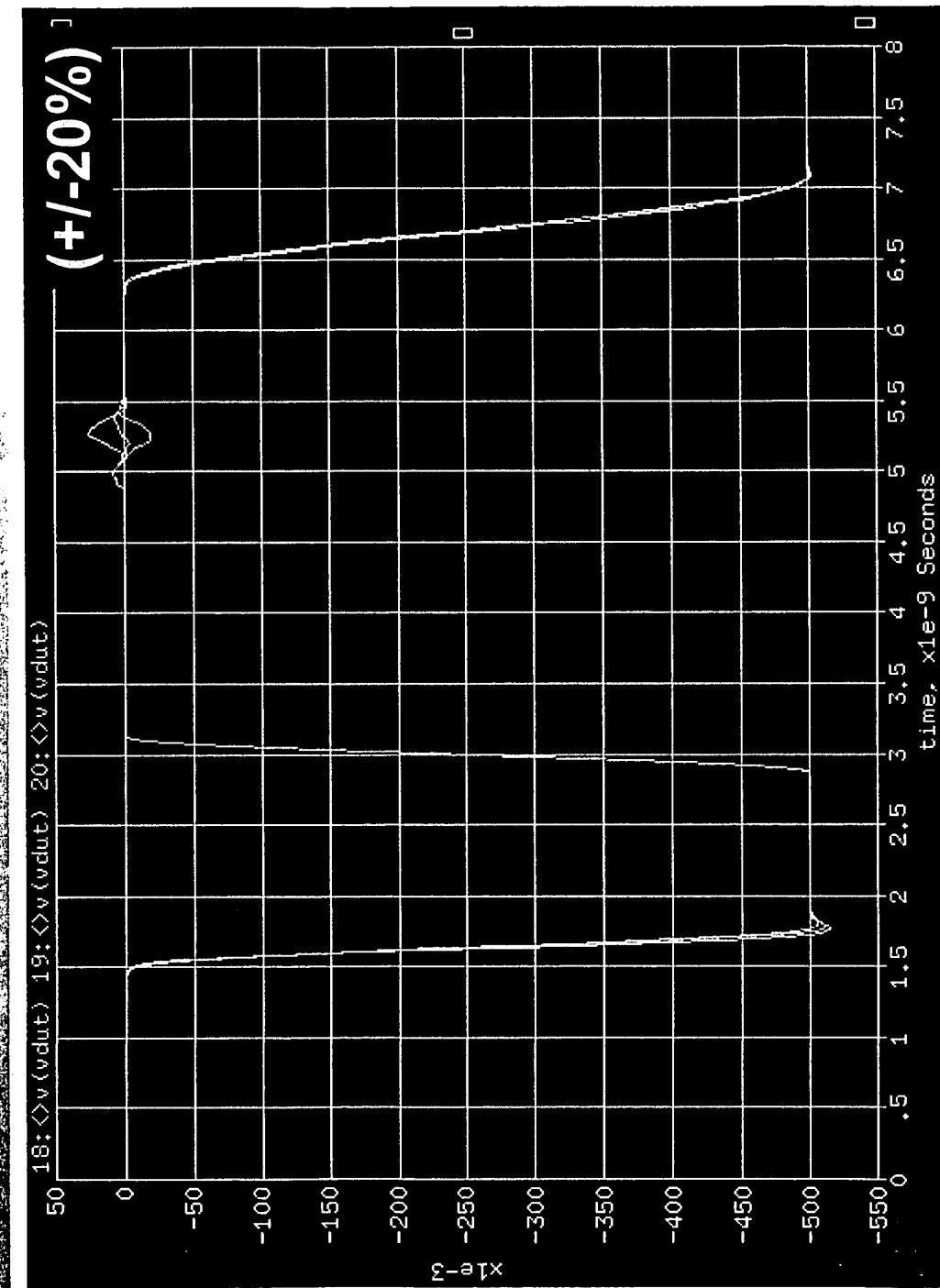
Sensitivity To Comparator Capacitance

Composite Overview Waveform at DUT - Reflection



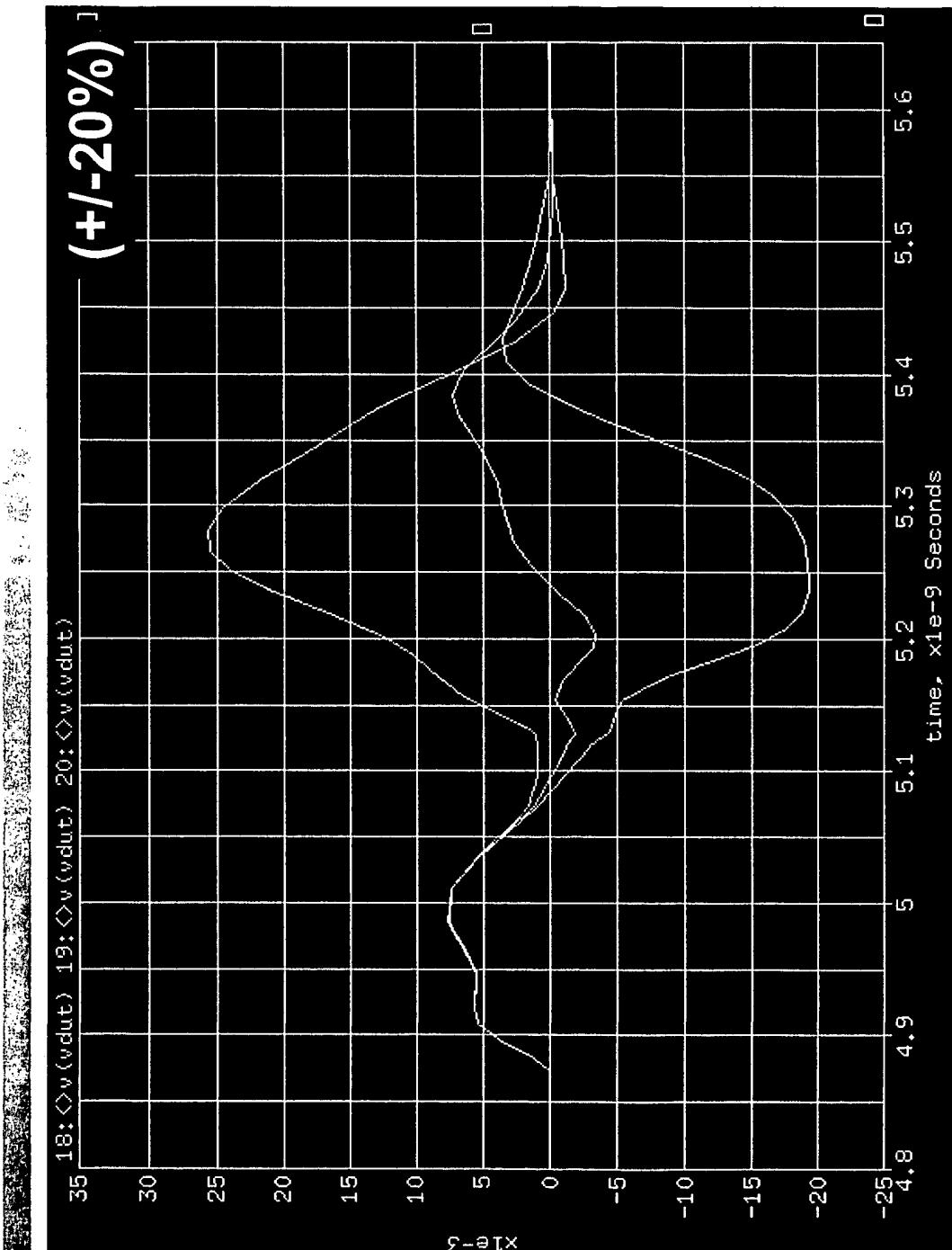
Sensitivity To A-Driver Capacitance

Composite Overview Waveform at DUT



Sensitivity To A-Driver Capacitance

Composite Overview Waveform at DUT - Reflection

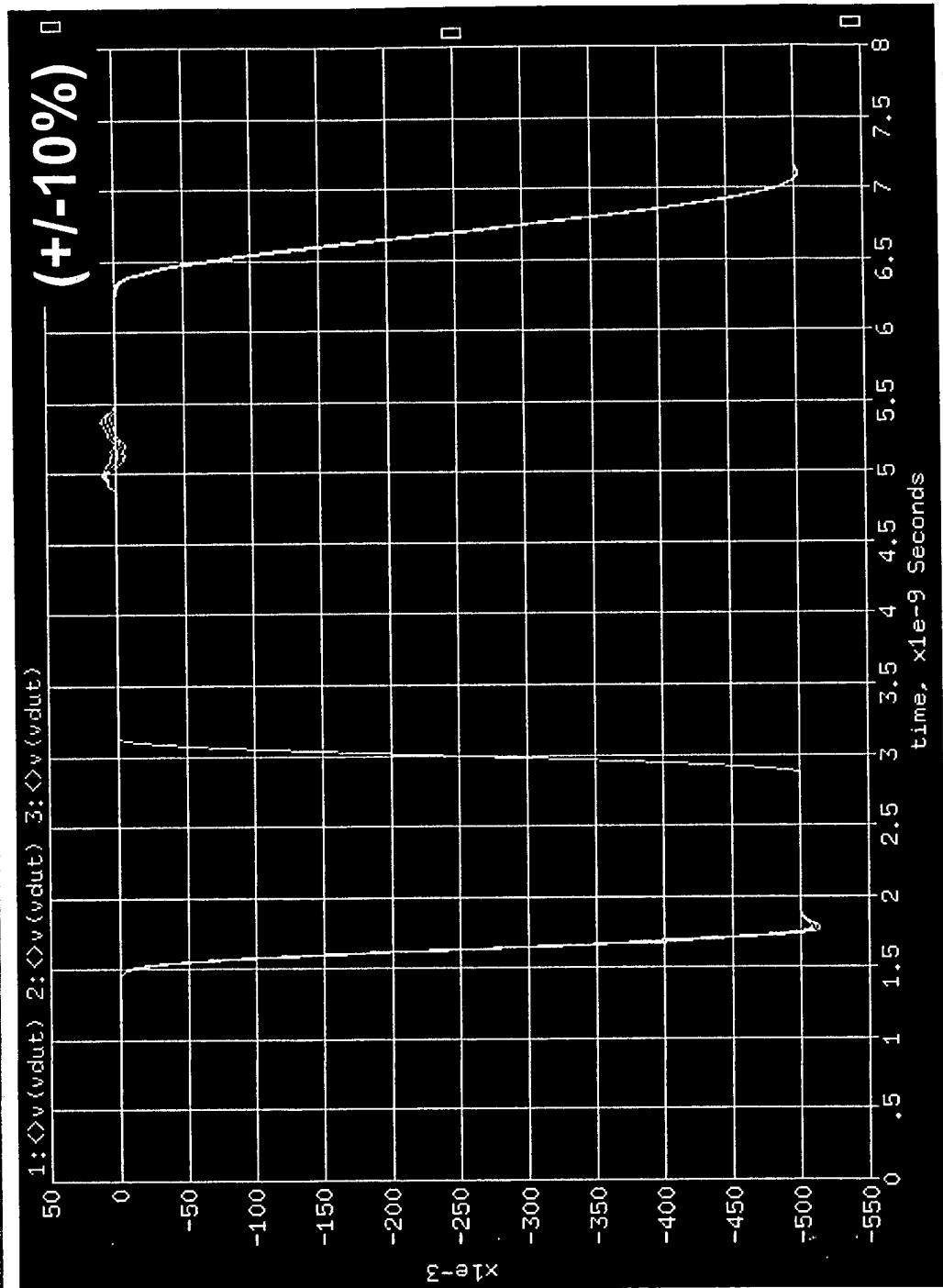


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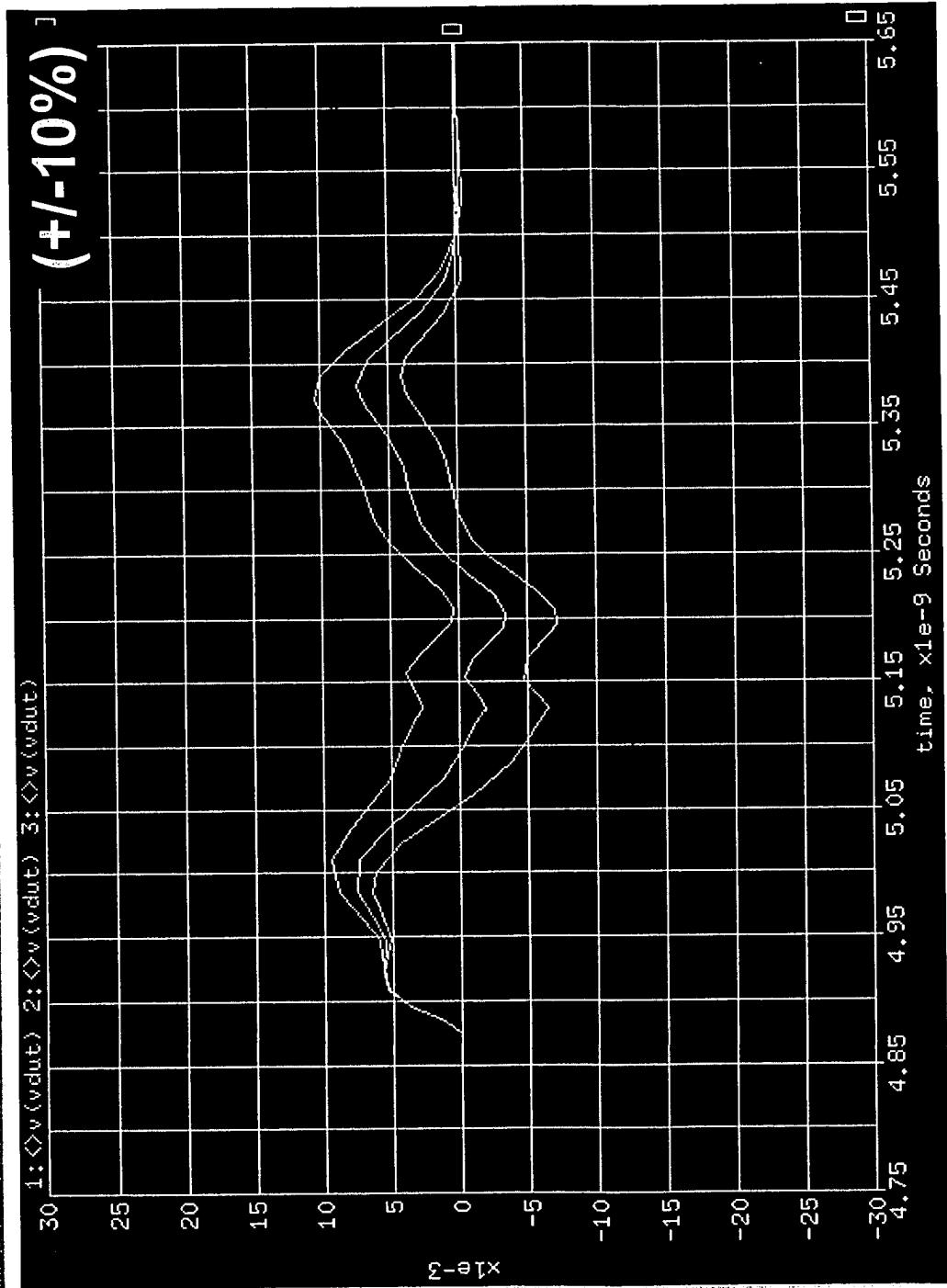
Sensitivity To Parasitic Capacitance

Composite Overview Waveform at DUT



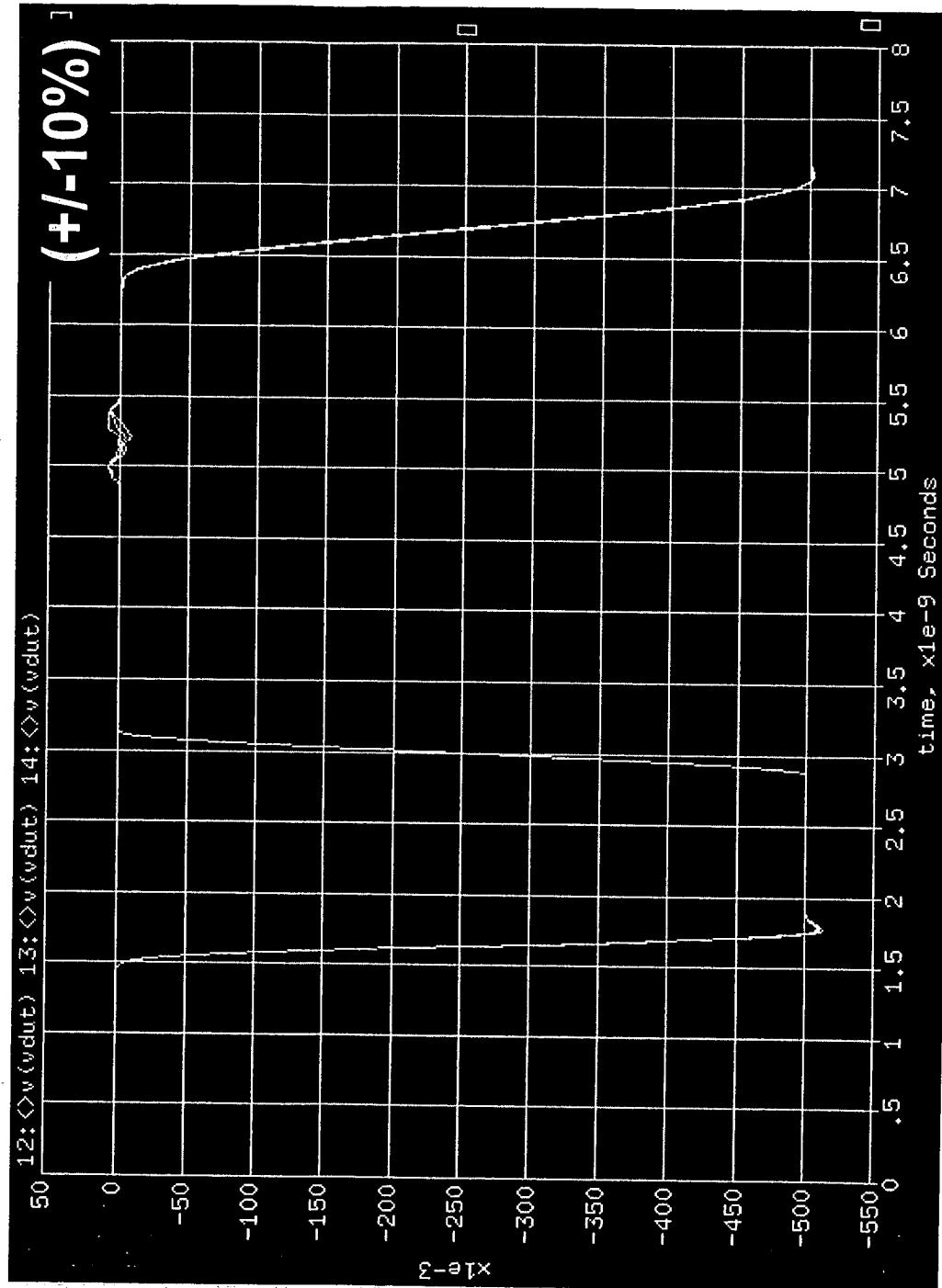
Sensitivity To Parasitic Capacitance

Composite Overview Waveform at DUT - Reflection



Sensitivity To Coupling Coefficient

Composite Overview Waveform at DUT

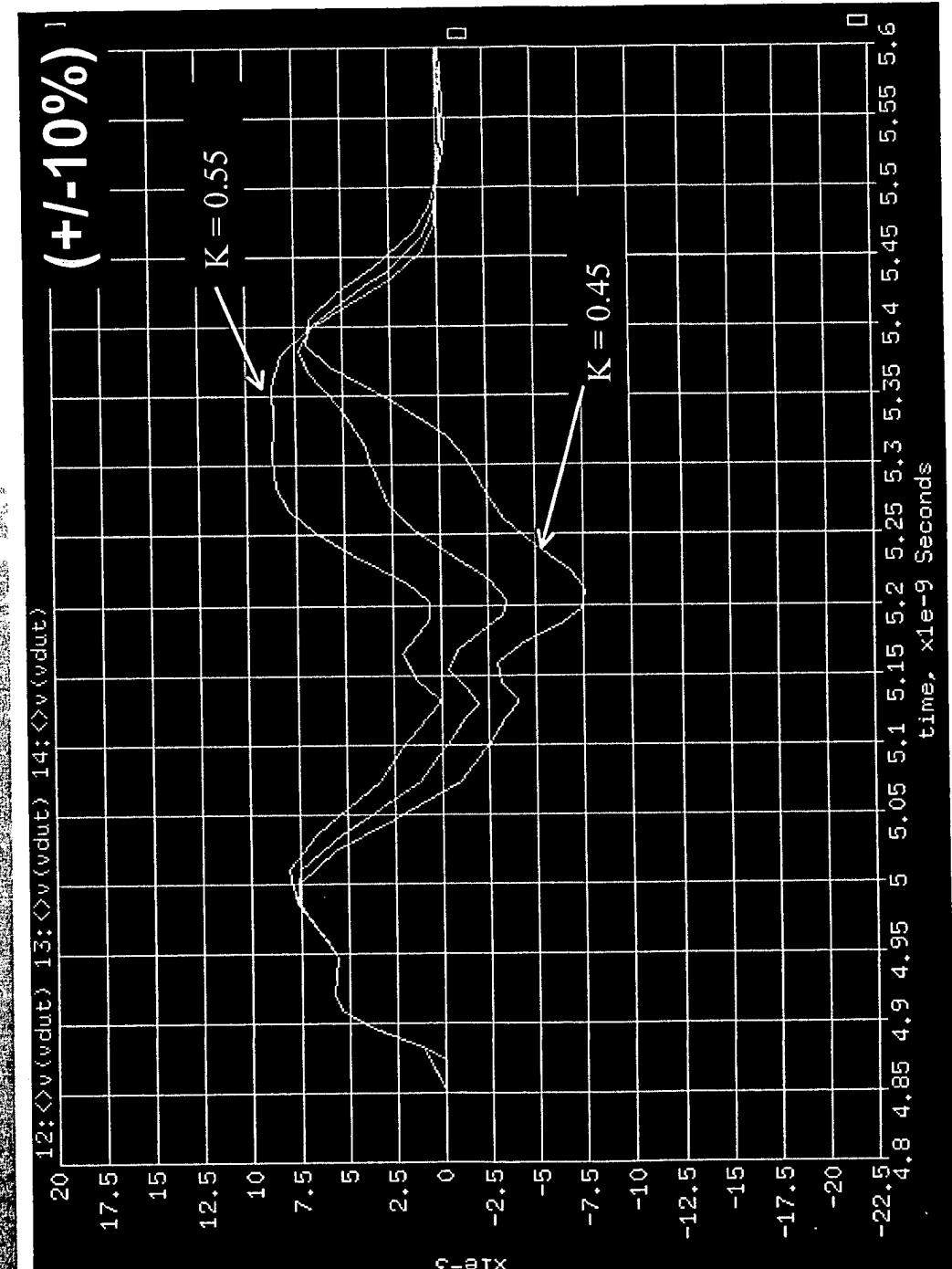


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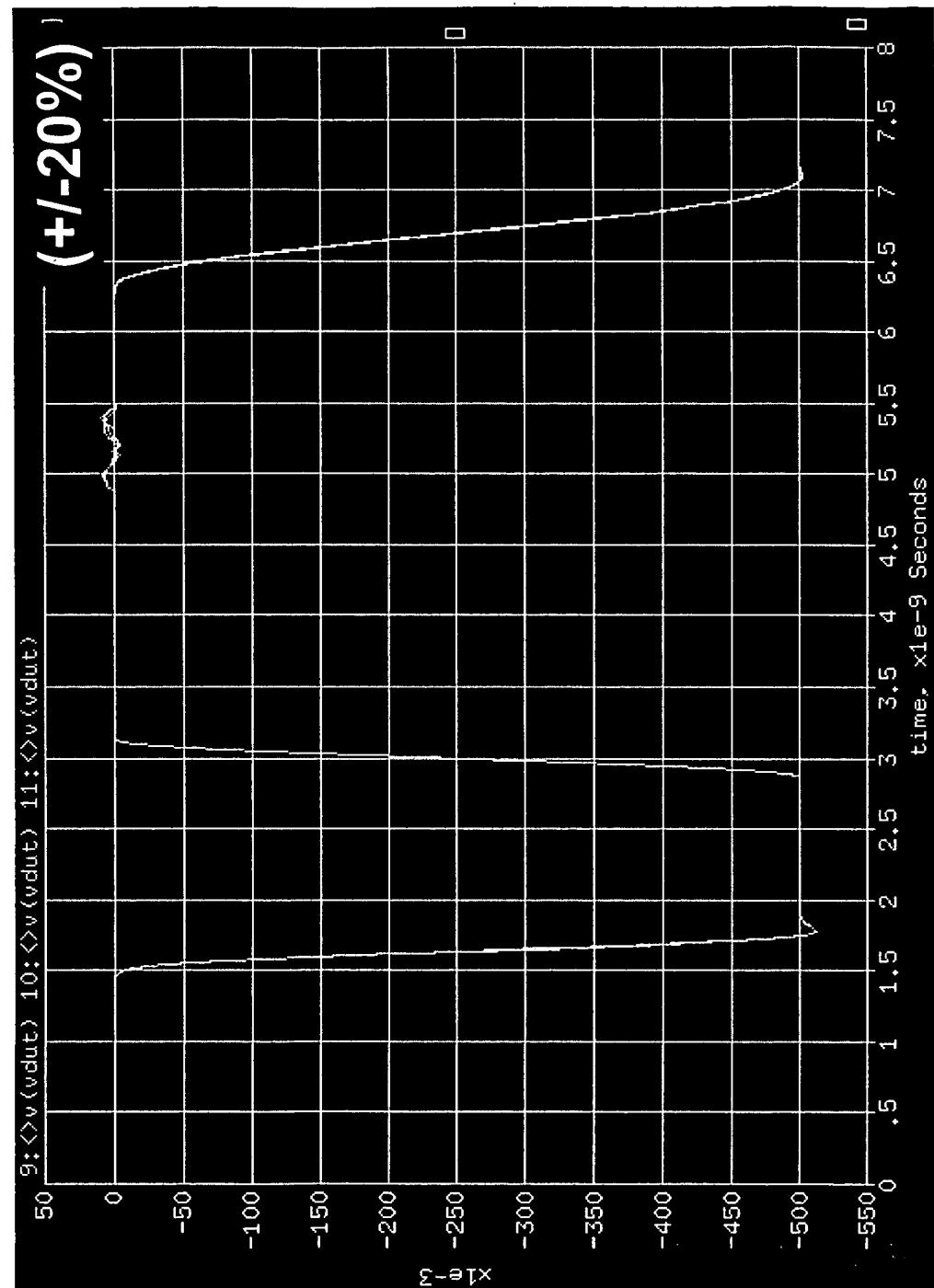
Sensitivity To Coupling Coefficient

Composite Overview Waveform at DUT - Reflection



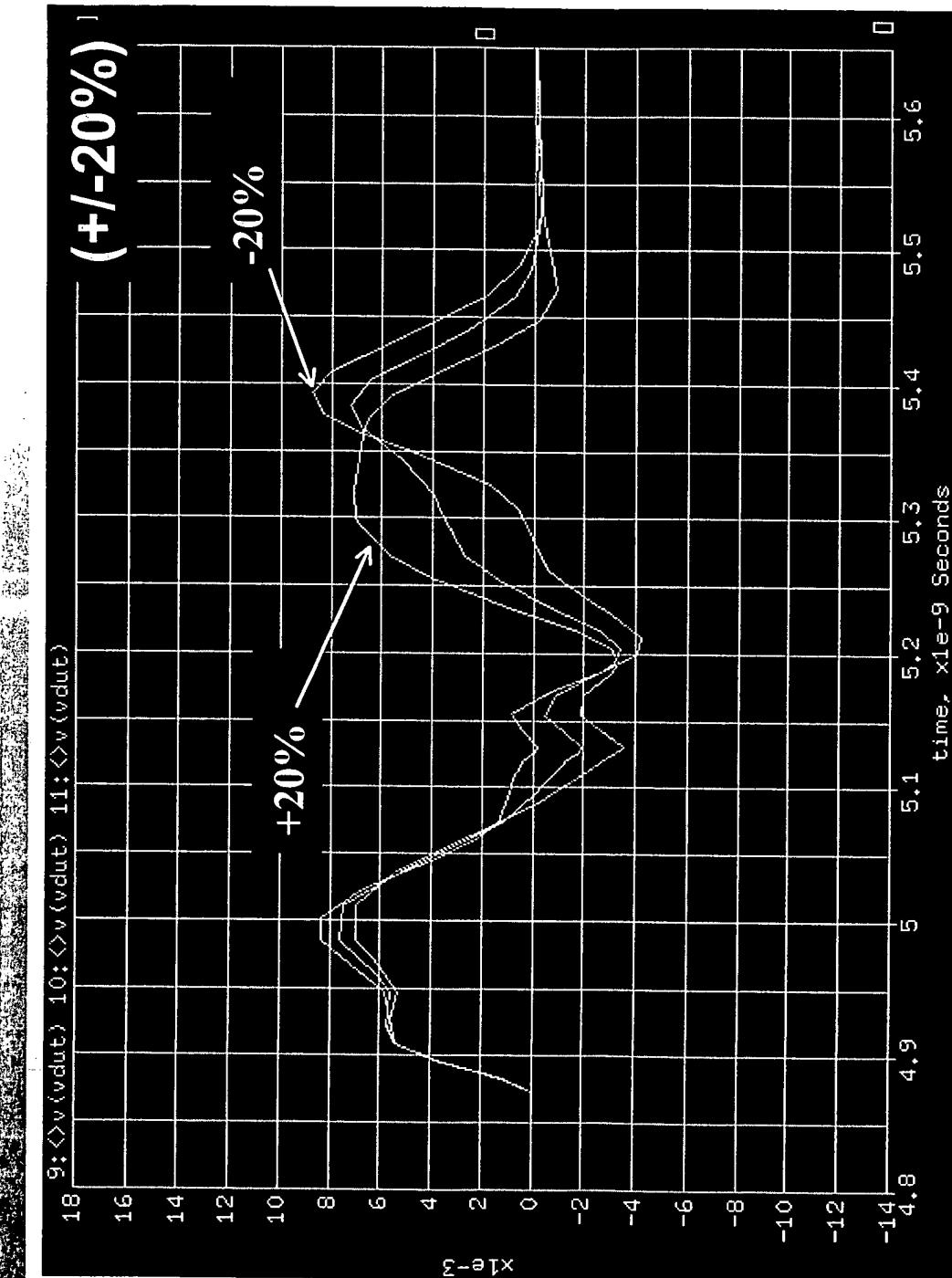
Sensitivity To Bridge Capacitor Value

Composite Overview Waveform at DUT



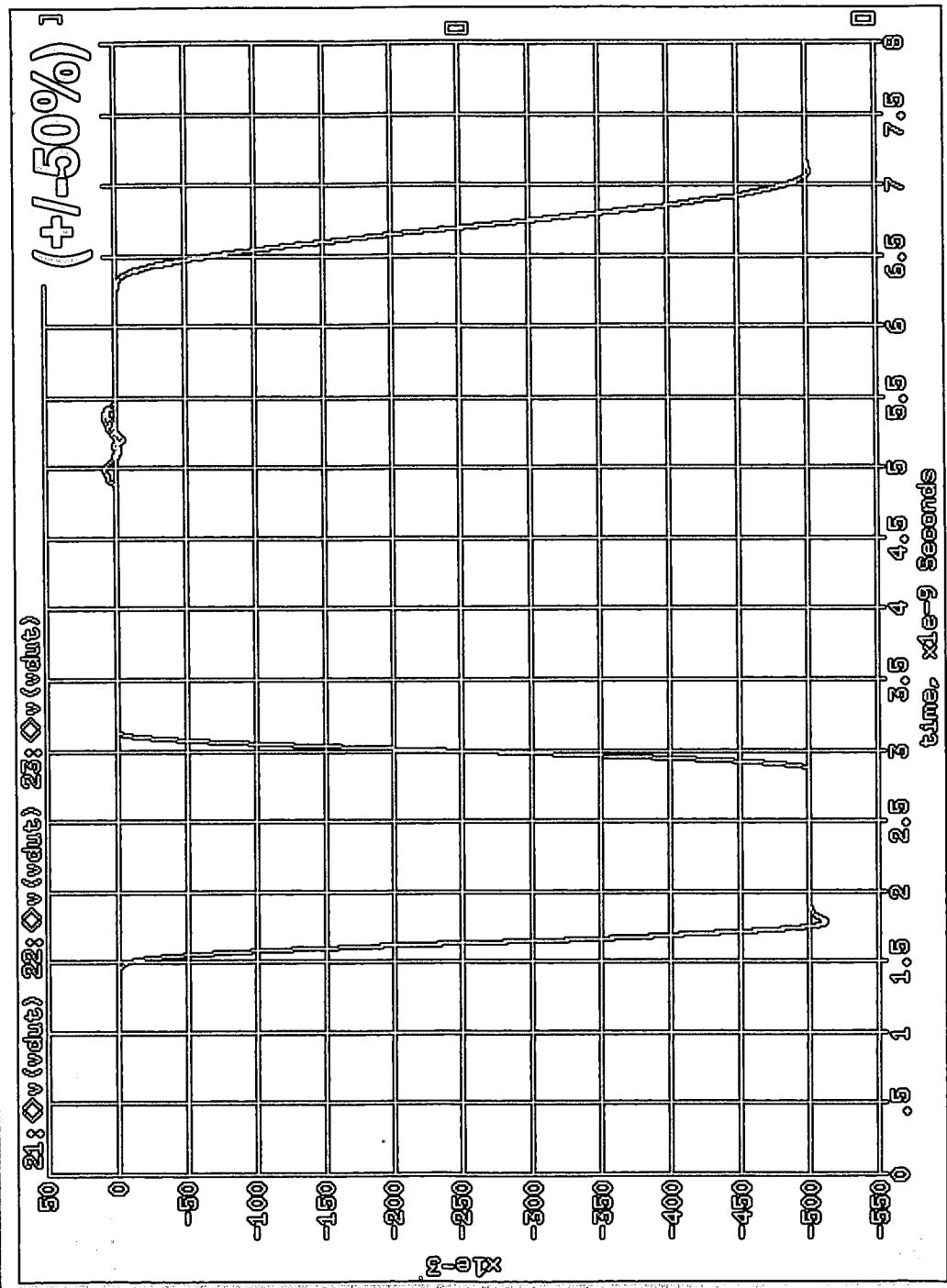
Sensitivity To Bridge Capacitor Value

Composite Overview Waveform at DUT - Reflection



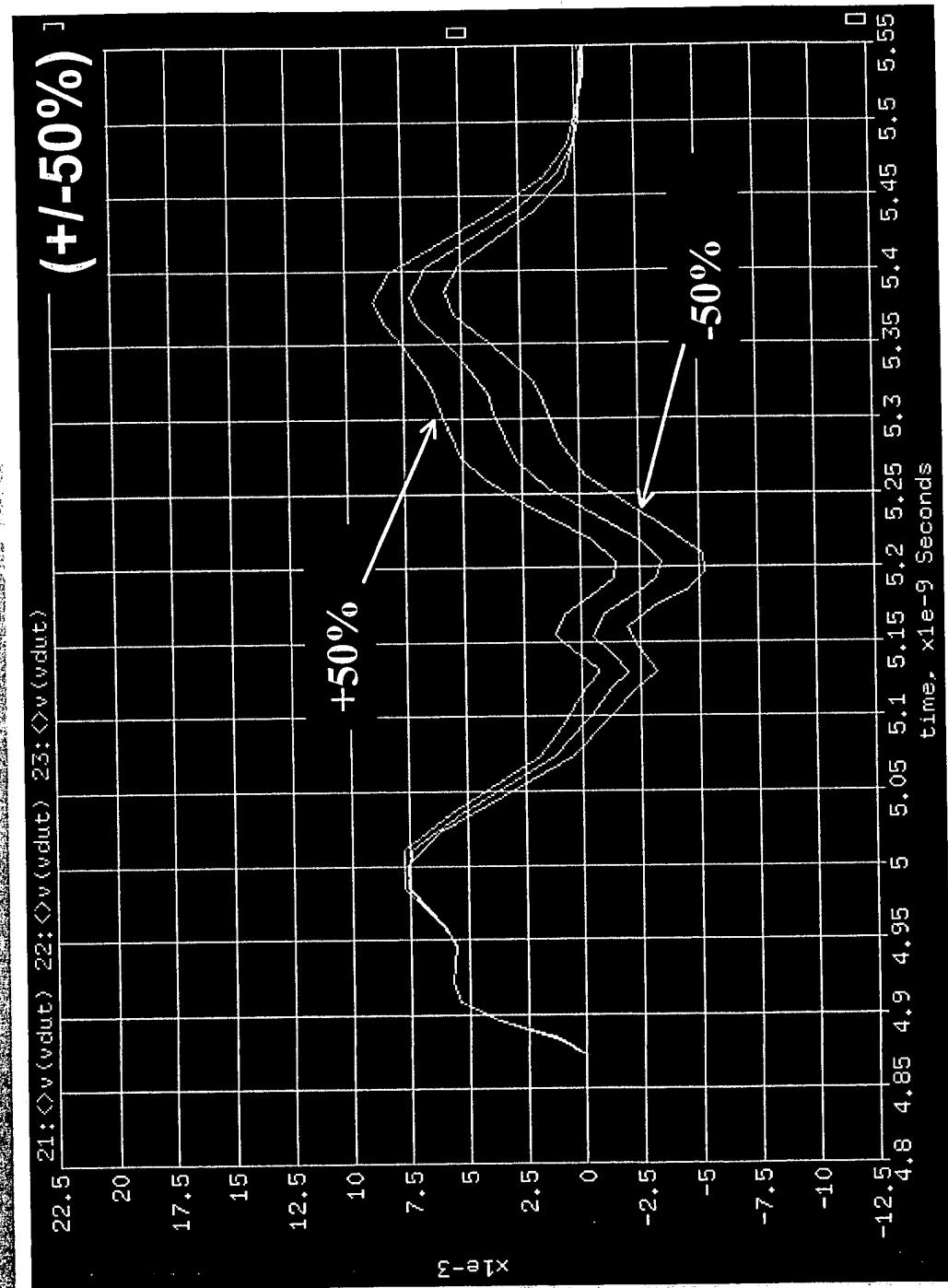
Sensitivity To Coil And Trace Resistance

Composite Overview Waveform at DUT



Sensitivity To Coil And Trace Resistance

Composite Overview Waveform at DUT - Reflection



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Chip Layout Overview

■ Preliminary - Work in Progress

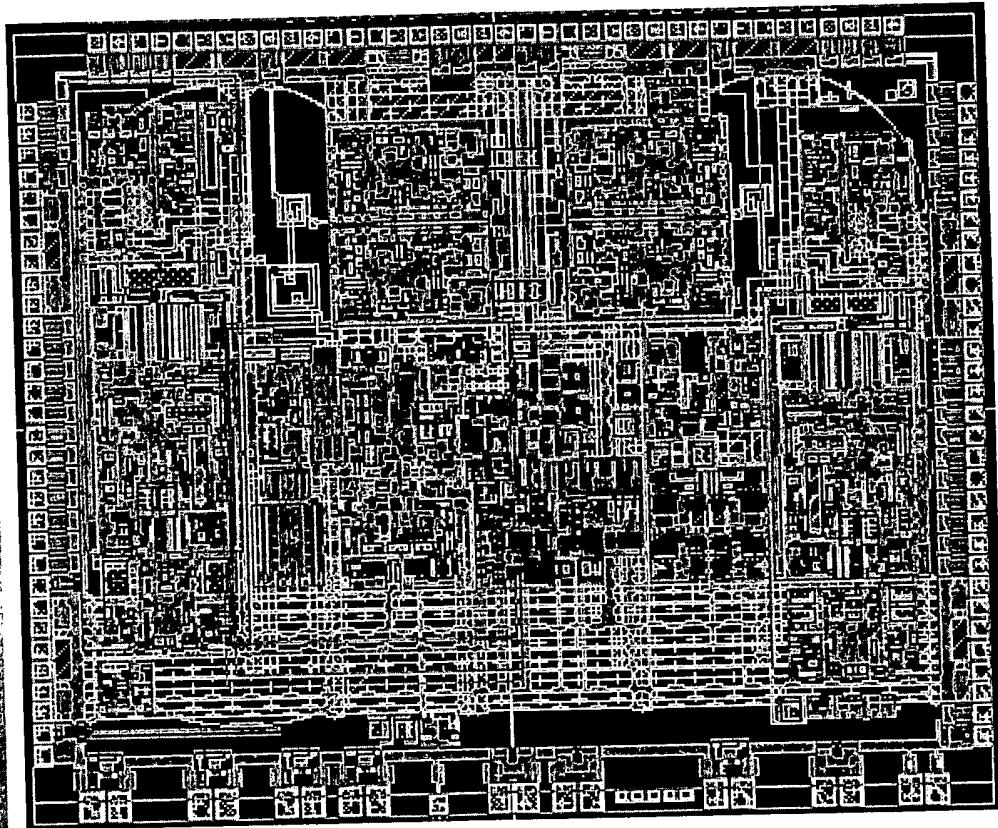


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Chip Layout: T-Coil Area Enlarged

Preliminary - "Artist's Conception" of T-Coils

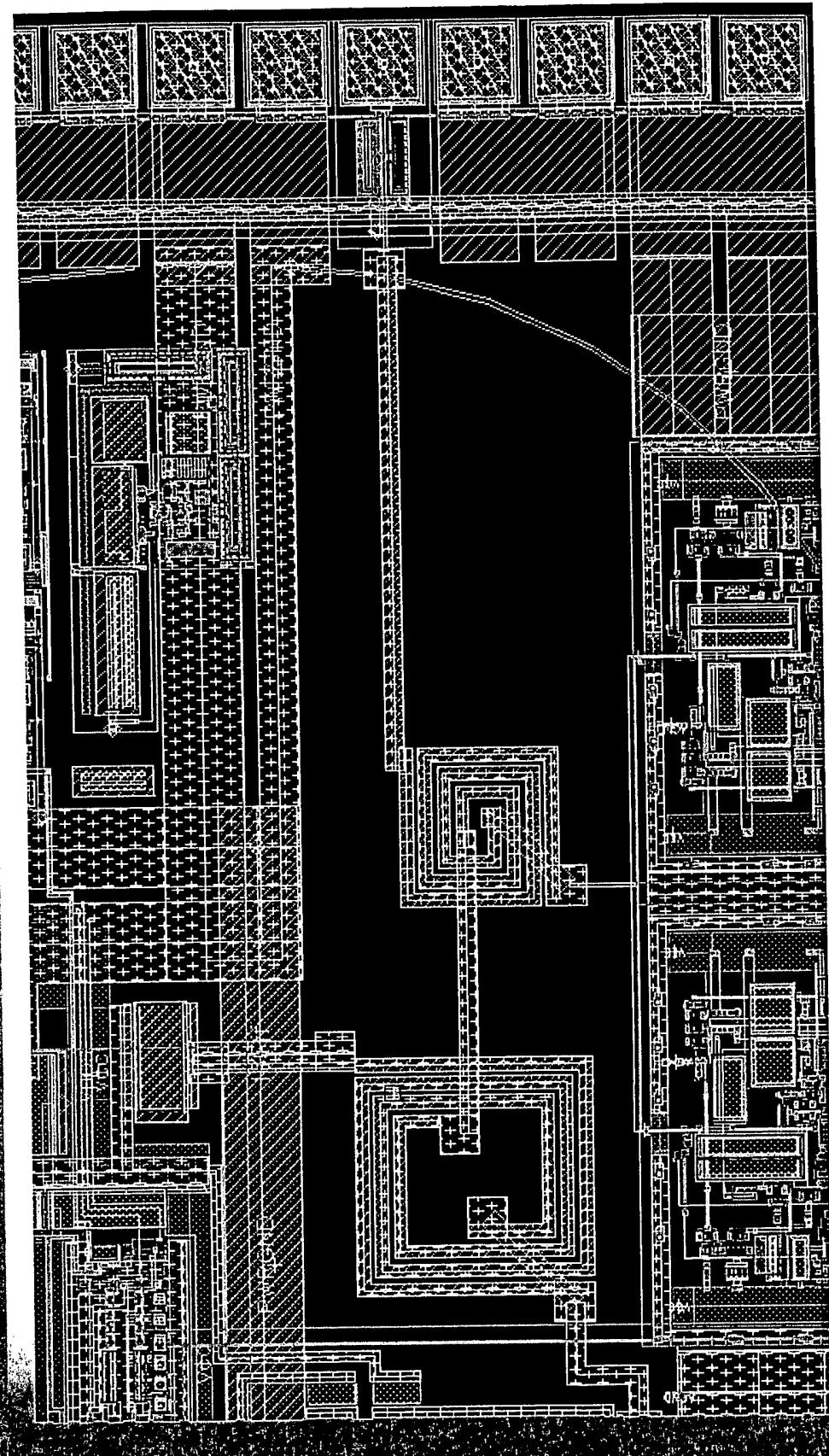


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Preliminary Actual Coil Layouts

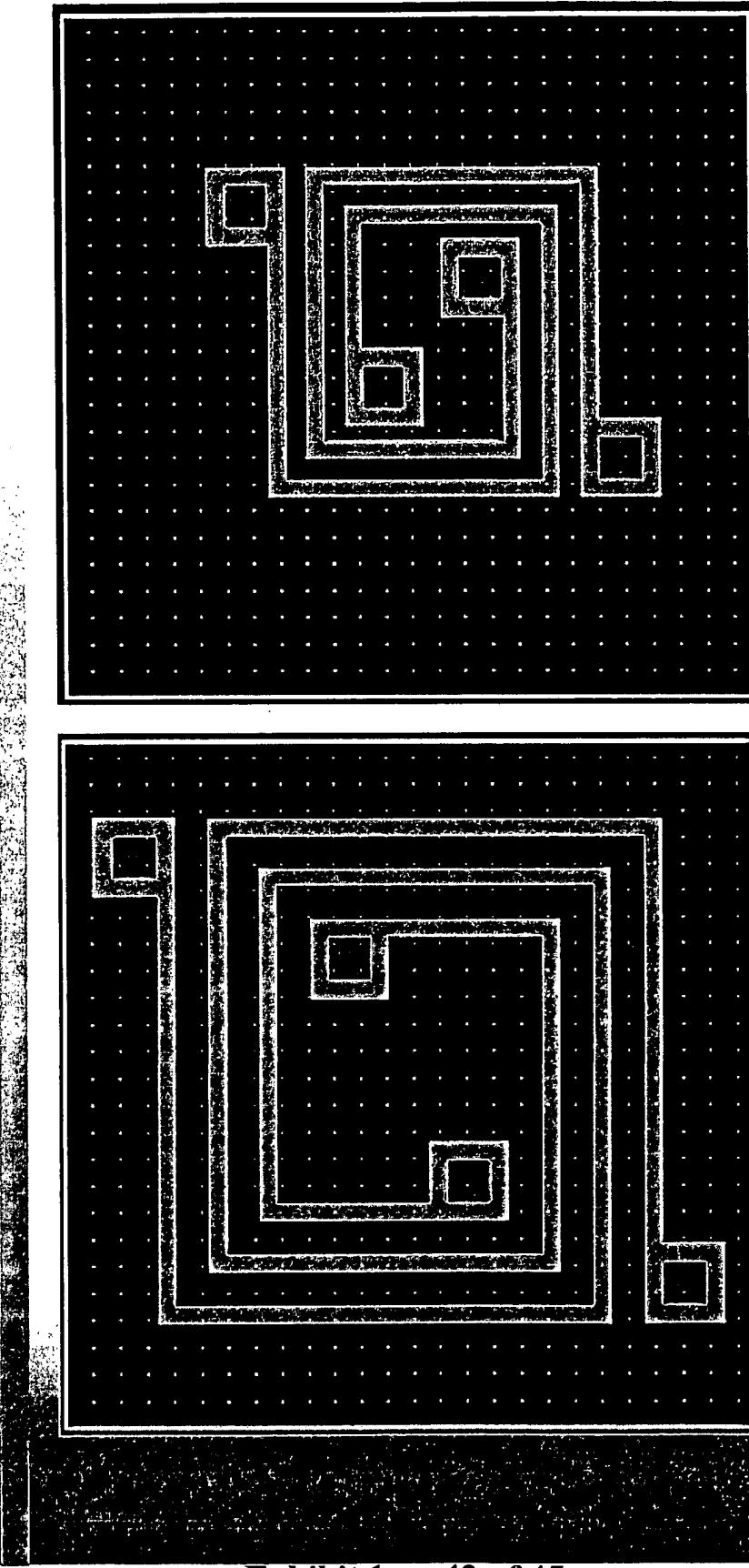


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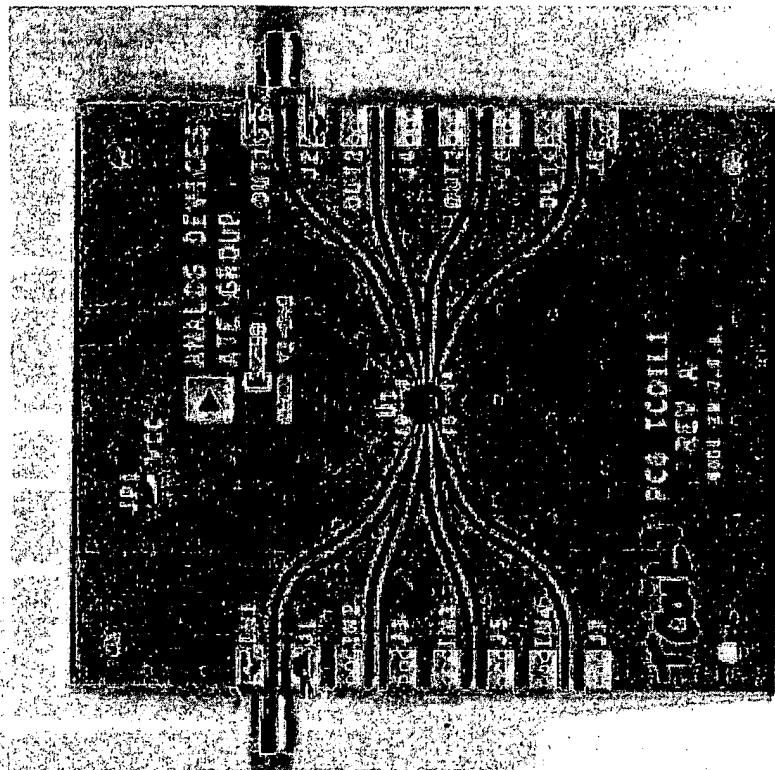
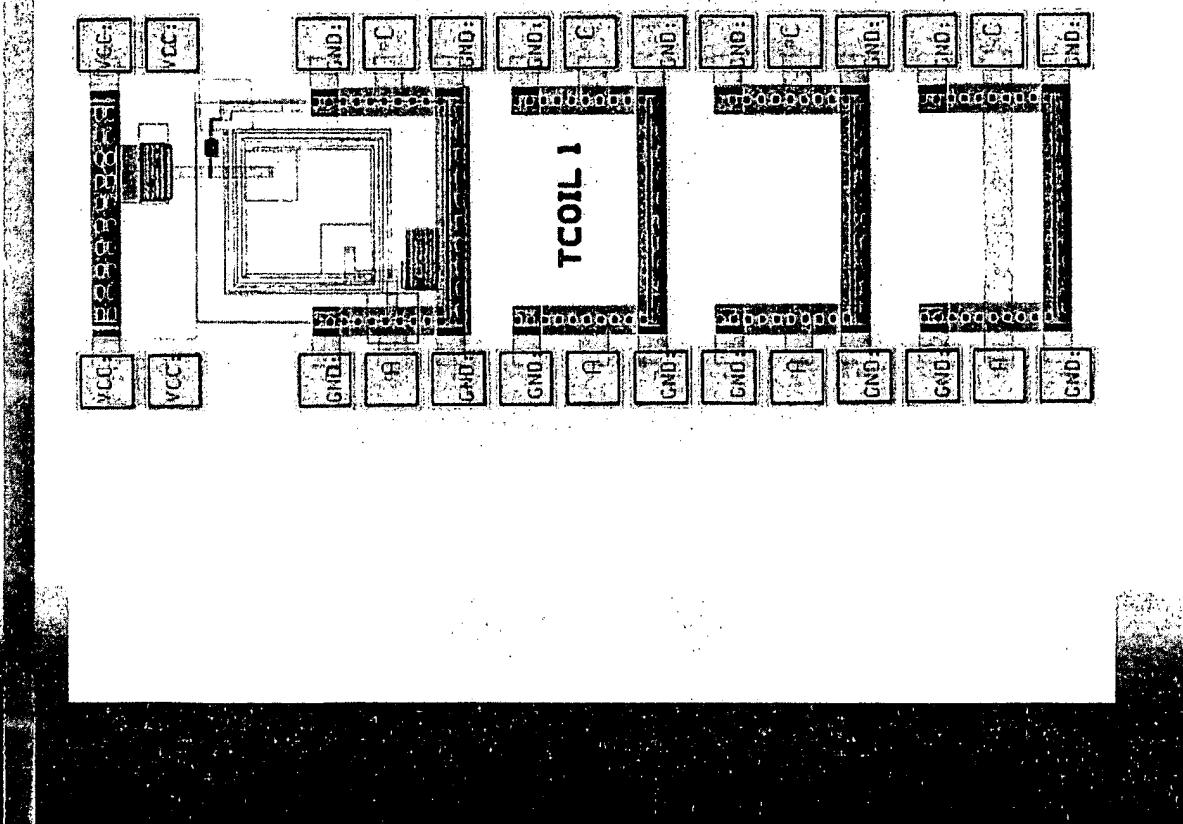
Where To Go From Here

- Finish Chip Layout
- Recalculate Values Based On Final Layout - Adjust Values As Required
- FAB IC
- Post-Process Coils At Multiple Suppliers
- Verify Models Through Characterization Of IC
- Gather Data For Process Spread Analysis
- Verify Reliability Through Qualification Process

Thanks To.....

- Doug Babcock
 - For the Original Ideas And Experience With T-Coils
- The UMIC Group
 - For Continued Support And.....
 - Letting Us Believe It May Actually Be Possible

METAL 3 INDUCTOR / TCOL STUDY



Boards: Bob Bombara

Build: John Dixon

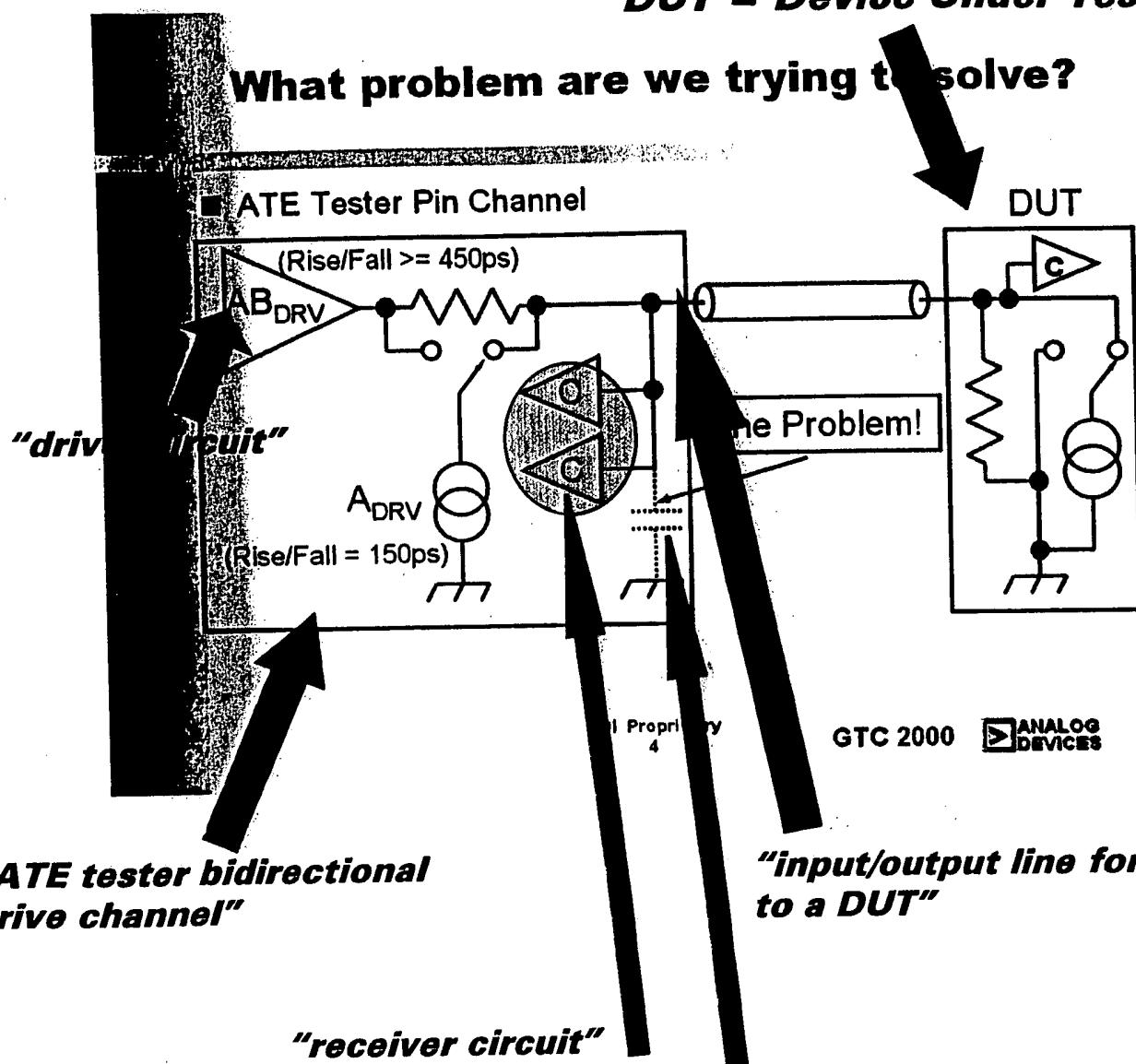
Bonding: Rick Sullivan

Layout: Jack Mason, Joe Zagami

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"DUT = Device Under Test"

What problem are we trying to solve?



"first passive matching network to at least partially compensate for receiver circuit capacitance"

How Do We Compensate?

Inductors

(Rise/Fall $\geq 450\text{ps}$)

AB_{DRV}

(Rise/Fall = 150ps)

A_{DRV}

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"voltage-mode driver circuit"

"current-mode driver circuit"

"ATE tester bidirectional drive channel"

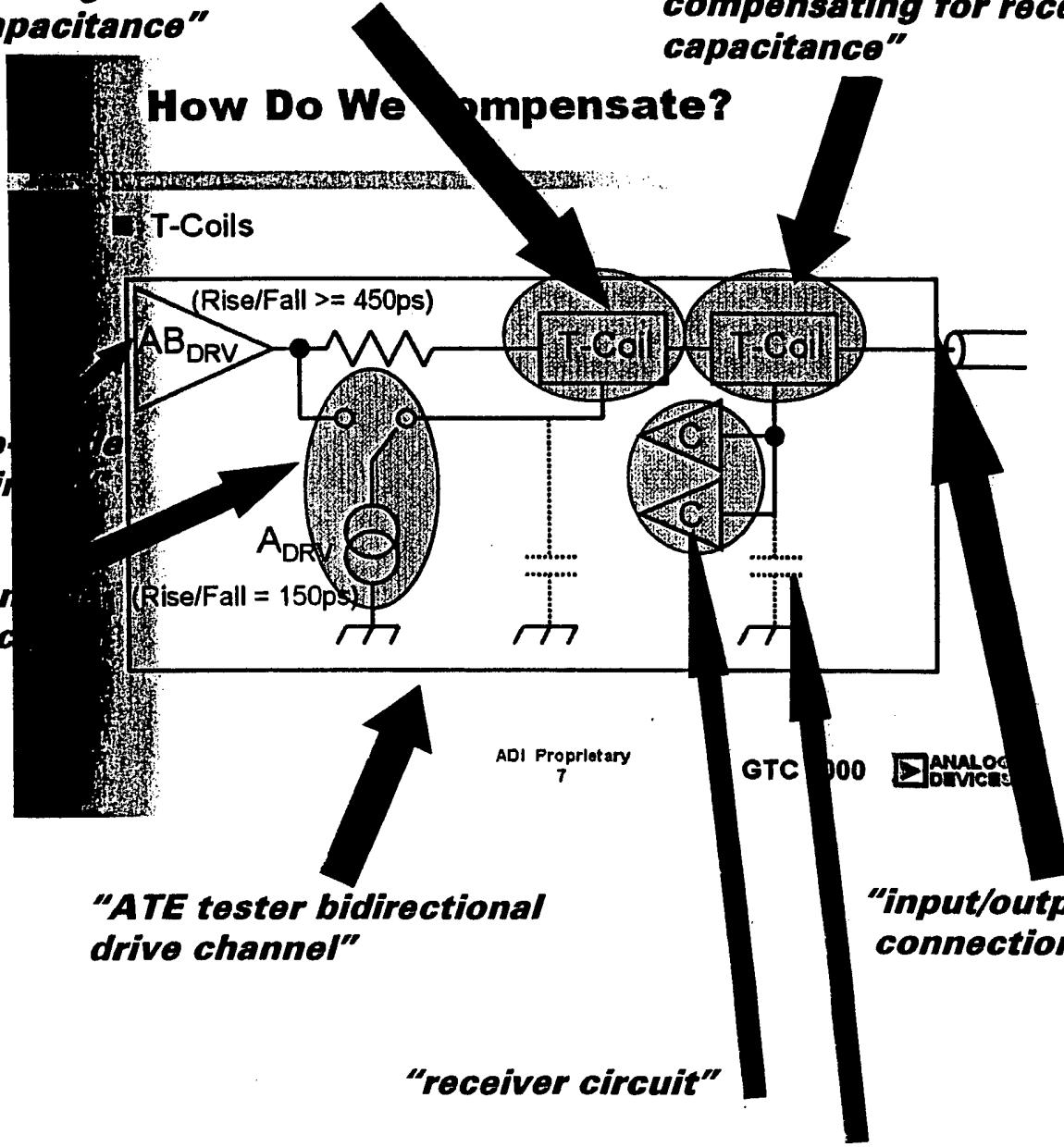
"input/output line for connection to a DUT"

"receiver circuit"

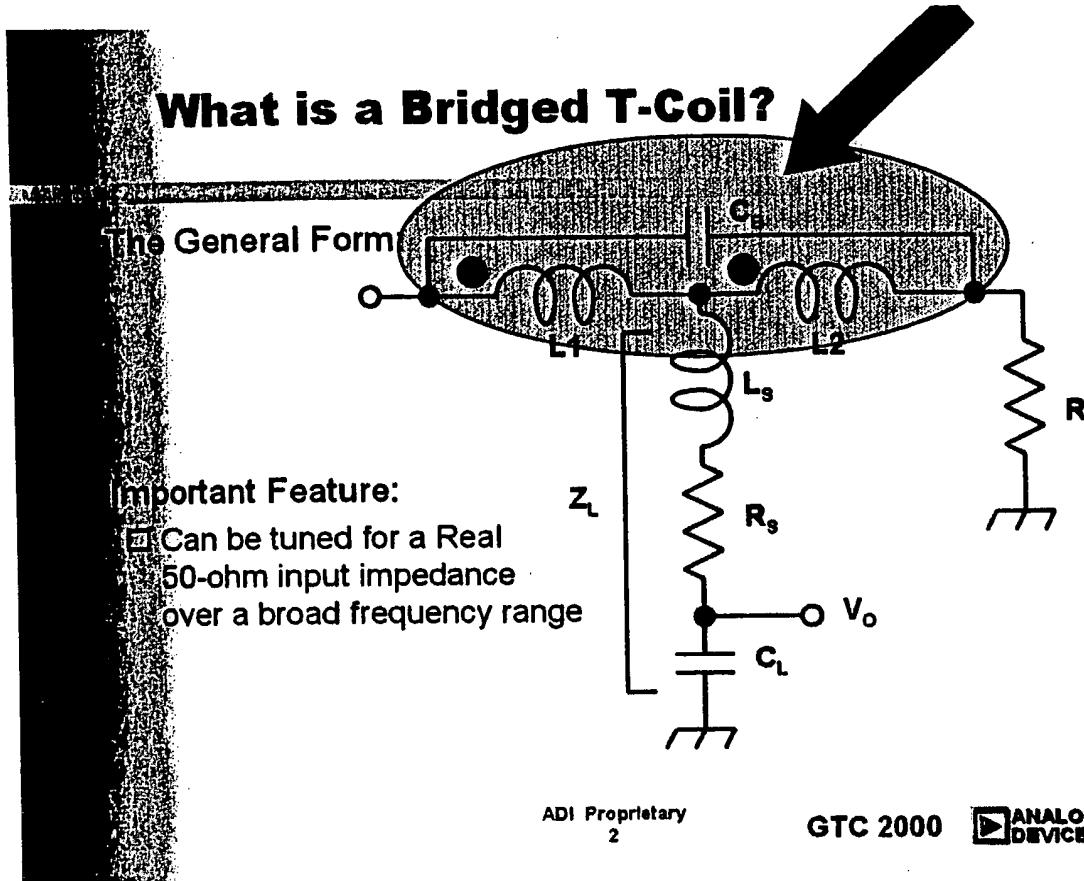
"associated capacitance of receiver circuit"

"second passive matching network, comprising a T-Coil circuit, compensating for current-mode driver capacitance"

"first passive matching network comprising a T-Coil circuit, compensating for receiver capacitance"



**"first passive matching network,
comprising a T-Coil circuit"**

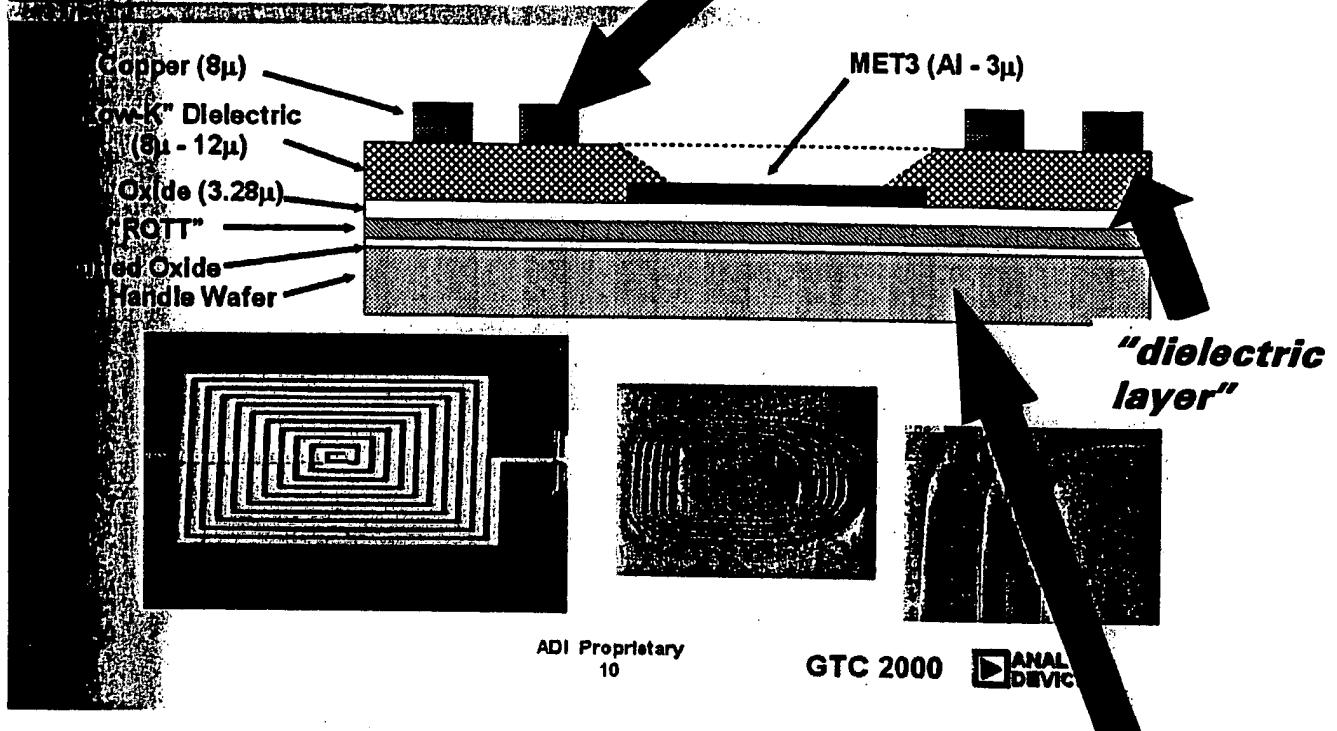


The T-coil circuit is formed by the transformer coupled-inductors, L1 and L2. The dots to the left of the coil symbol indicate the magnetic flux through the coils are linked in the polarity indicated. C_B is the bridging capacitor.

The elements L_s , R_s represent the circuit elements of series inductance and series resistance connecting the T-Coil circuit to the load capacitance C_L . In the case of the ATE Pin Electronics system, this could be the receiver associated capacitance.

"T-coil inductors implemented in a separate layer"

What Do The Post-Processed Structures Look Like?

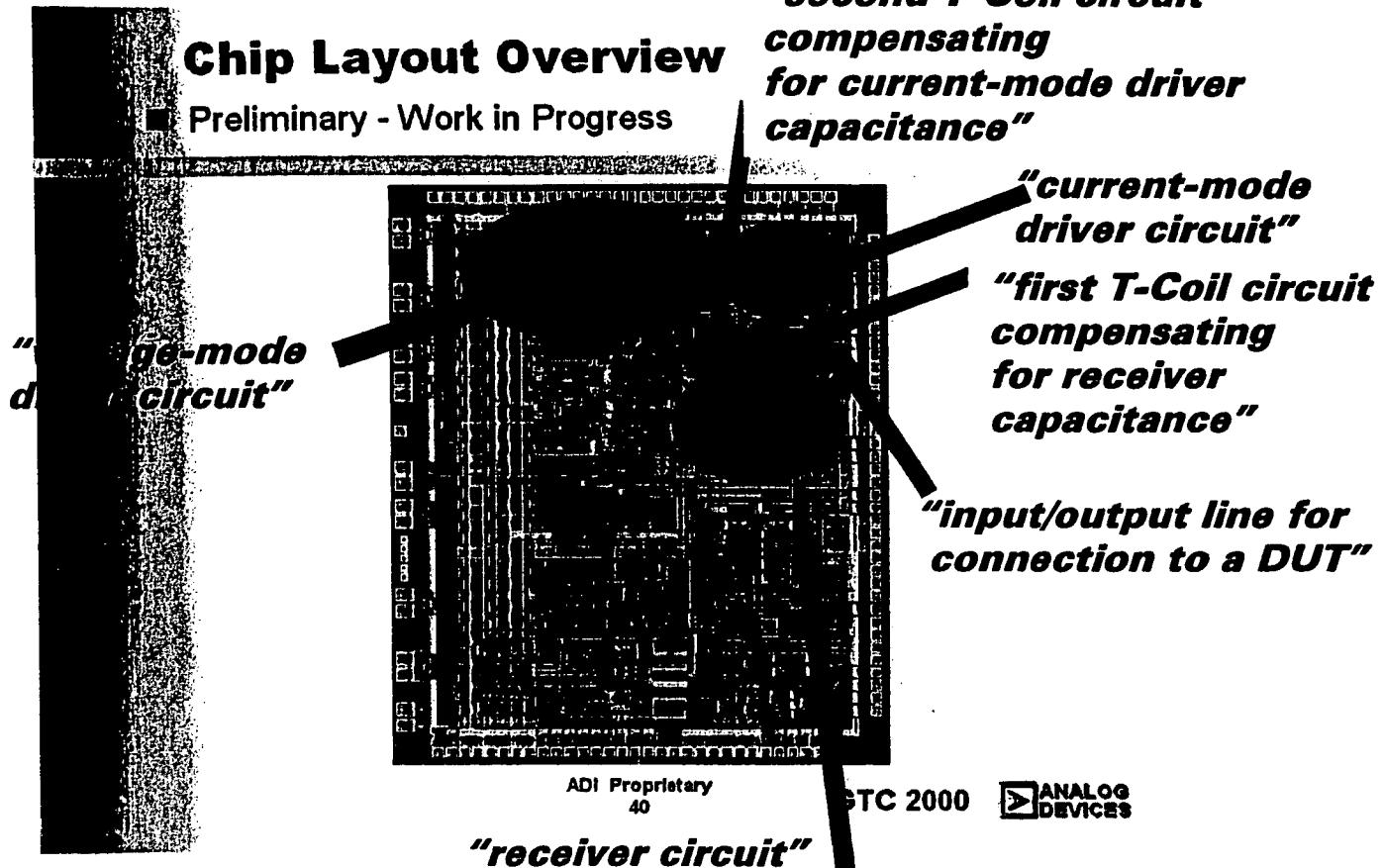


"common layer of an integrated circuit (IC)"

Cross section showing T-Coil transformer coils implemented in a separate layer of an IC that is spaced from the common layer by at least a dielectric layer.

Chip Layout Overview

■ Preliminary - Work in Progress



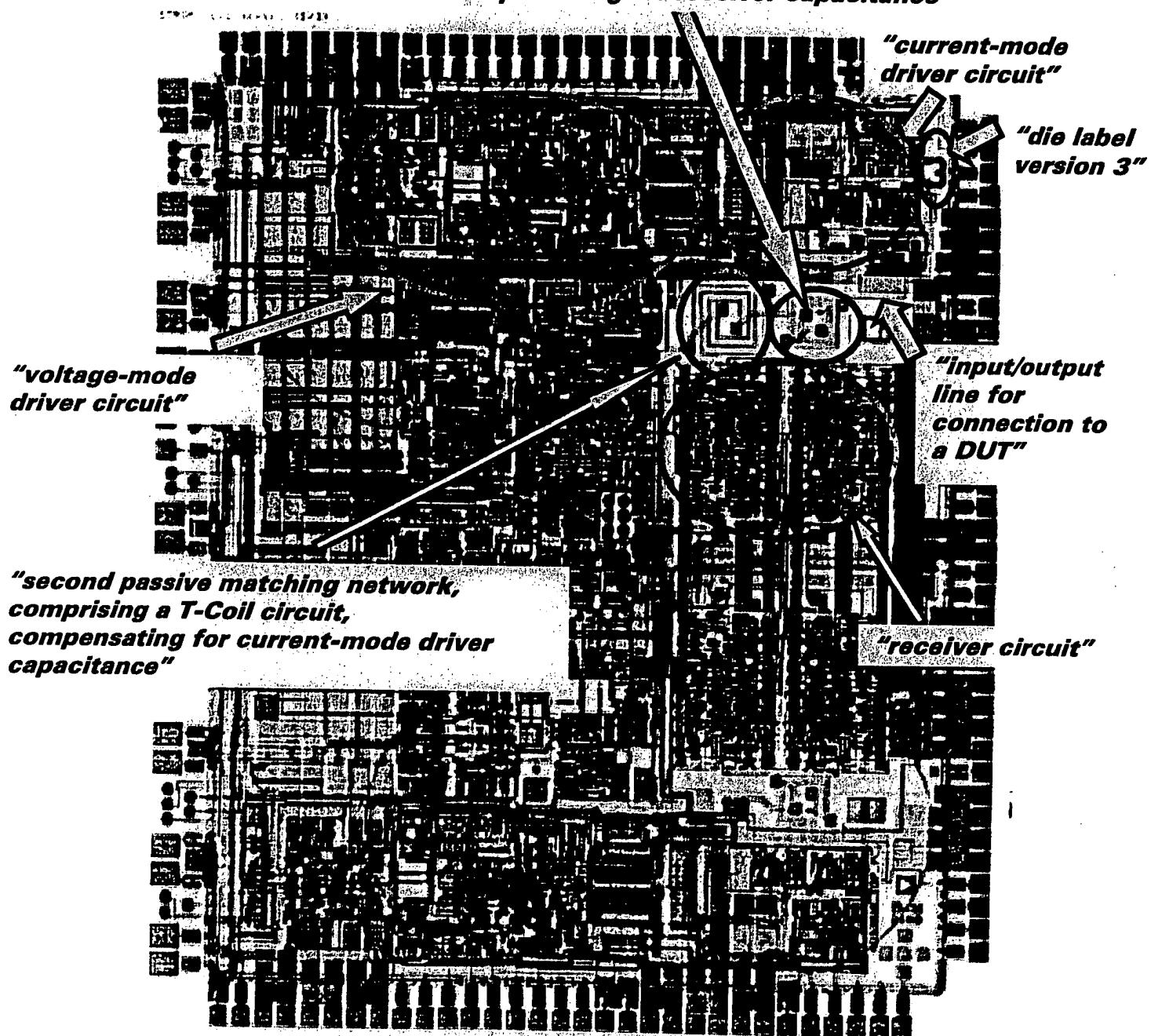
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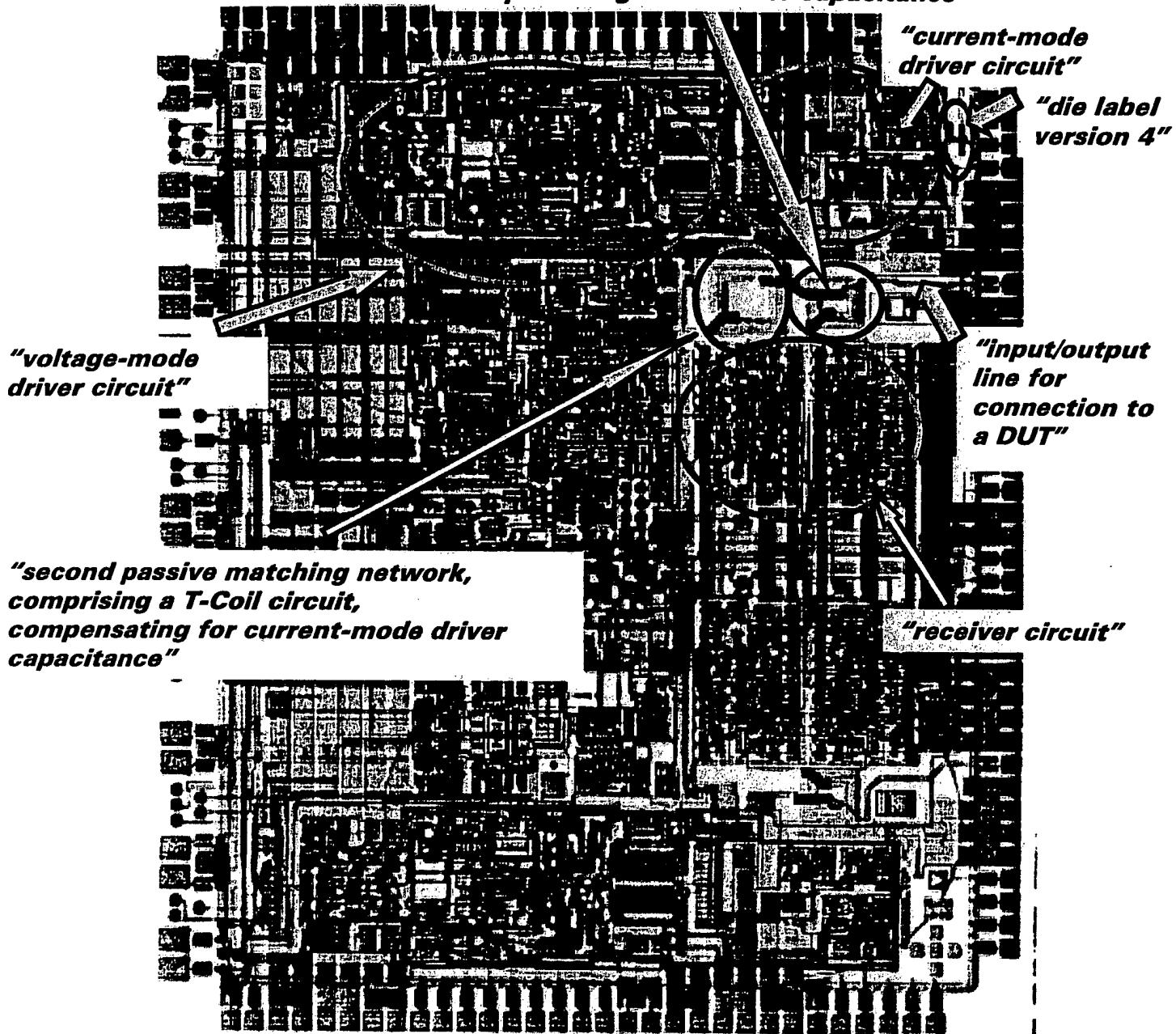
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Integrated circuit layout plot showing driver, receiver, input/output line, and T-Coils.

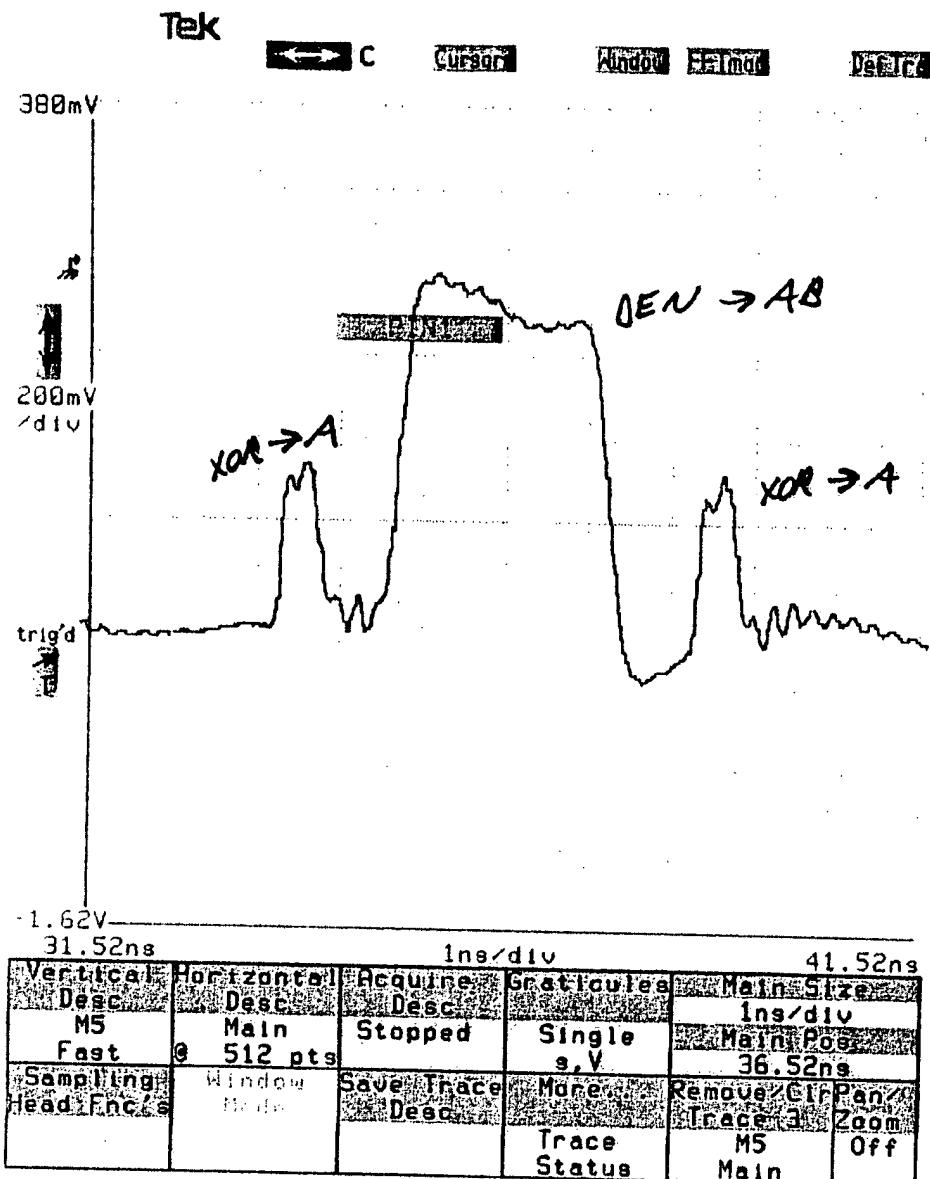
*"first passive matching network,
comprising a T-Coil circuit,
compensating for receiver capacitance"*



***"first passive matching network,
comprising a T-Coil circuit,
compensating for receiver capacitance"***



11801C DIGITAL SAMPLING OSCILLOSCOPE
date: 22-AUG-00 time: 20:13:26



Measurement of functional operation of ad53510pc silicon, August 22, 2000
showing current-mode driver (A) and voltage-mode driver (AB) operation.

First Samples Ad53510-PC

Wafer 637980-5

Trimmed 20-Sep-2000

Program is archived in

doc: /cts5000/home/eng/ad53510_archive/1stSample_092000
alltestcode_1stSample_092000.tar.Z

637980_5_ad53510PC_trm_doc_092000_184151.stdf

Site 1 Version 0 Yield 8/24

...Tweaked SLRD trim geometry, opened up test limits to improve yield.

637980_5_ad53510PC_trm_doc_092000_182850.stdf

Site 2 Version 0 Yield 15/20

Die stepping misaligned because find_first_die targets
in vs_align2.dat were incorrect; first 9 tested were all bin-1's
but were not marked because gv_trm_scratch_pad was off;
walked off wafer after #20, then program crashed & needed ^X;

637980_5_5_ad53510PC_trm_doc_092000_181452.stdf

Site 2 Version 0 Yield 2/3

Manually wrote to scratchpad 1st 9 sites (#1,201 thru 1,209)

Set gv_wafer_num to 5 for die tested in this .stdf

637980_5_ad53510PC_trm_doc_092000_170844.stdf

Site 3 Version 0 Yield 19/24

637980_5_ad53510PC_trm_doc_092000_162647.stdf

Site 9 Version 4 MET-3 T-COILS Yield 17/24

Limit File: 637980_5_ad53510PC_trm_doc_092000_184151.stdf

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_184151.stdf

Tester: CMS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Std Ver: 4 Cpu: 1

Prober: Operator: eng

Job: /prod/dfst.load Lot: 637980 Sublot: Tested: 24 Pass: 17 Yield: 70.83%

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_182850.stdf

Tester: CMS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Std Ver: 4 Cpu: 1

Prober: Operator: eng

Job: Lot: 637980 Sublot: Tested: 24 Pass: 19 Yield: 79.17%

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_181452.stdf

Tester: CMS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Std Ver: 4 Cpu: 1

Prober: Operator: eng

Job: Lot: 637980 Sublot: Tested: 3 Pass: 2 Yield: 66.67%

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_170844.stdf

Tester: CMS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Std Ver: 4 Cpu: 1

Prober: Operator: eng

Job: /prod/dfst.load Lot: 637980 Sublot: Tested: 20 Pass: 15 Yield: 75.00%

File Analyzed: 637980_5_ad53510PC_trm_doc_092000_162647.stdf

Tester: CMS 5010 Station: 1 Node: doc Exec: 5010_1.9.3e Std Ver: 4 Cpu: 1

Prober: Operator: eng

Job: /prod/dfst.load Lot: 637980 Sublot: Tested: 24 Pass: 8 Yield: 33.33%

Combined Lots Tested: 95 Pass: 61 Yield: 64.21%

Numb	Test Name	Valid	Stat Qty	Test Limits		Statistic Data Range		Mean	Units	Std Dev	Ulimit	Slimit	CPK	% Eve	Fail	Notes
				Min	Max	Min	Max									
1	REV_DATE	95	95	0	9999.99	92000.000	92000.000	-81.60	0	0.00	0	0.00	Inf	Inf		
2	perf_id	95	95	0	9.000000	0	0	-100.00	0	0.00	0	0.00	NaN	NaN		
3	board_id	95	95	0	9.000000	0	0	-100.00	0	0.00	0	0.00	Inf	Inf		
4	ring_id	95	95	0	9.000000	1.0000000	1.0000000	-77.78	0	0.00	0	0.00	Inf	Inf		
5	contact_id	95	95	0	9.000000	1.0000000	1.0000000	-77.78	0	0.00	0	0.00	Inf	Inf		
20	al_die_align_PASSE	95	95	-0.9000000	0.9000000	0	0	0.00	0	0.00	0	0.00	Inf	Inf		
10	Opens Continuity	95	95	Pass	Fail	Pass	Fail	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
11	Short Continuity	95	95	Pass	Fail	Pass	Fail	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
12	PadNum Continuity	95	95	Pass	Fail	Pass	Fail	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
13	PinNum Continuity	95	95	Pass	Fail	Pass	Fail	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
14	EdgeSense_R	95	94	0	2500.0000	148.00000	293.00000	245.39362	-80.37	55.395977	2.22	1.48	1.05	1.05		
15	NCY7_R	95	94	0	4.0000000	-1.0000000	4.0000000	1.0000000	-50.00	1.7564471	43.91	*	0.19	1.05		
16	DieVersion	95	95	0	1.0000000	-1.0000000	4.0000000	1.0000000	8.08	10.580537	10.58		1.45	2.11		
17	TO_Pream	95	93	0	1.5000000	0.3500000	0.5000000	0.4136843	-67.13	0.0367873	2.83		1.94			
22	Laser Power_wJ	95	95	0.2000000	1.5000000	0.50731646	5411.3257	5170.0293	-13.20	62.738003	1.25		11.53	1.05		
24	TsnsR_Pream	95	94	3000.0000	8000.0000	5073.1646	5411.3247	5171.2314	34.25	62.644276	6.26		1.75	1.05		
25	TsnsR_Trimmed	95	94	4500.0000	5500.0000	5075.5205	5411.3247	5171.2314	34.25	62.644276	6.26		1.75	1.05		
26	R2_TrimIns	95	93	65.000000	75.000000	68.759850	72.039436	70.557480	11.15	0.5401545	5.40		2.74	2.11		
100	lvcc_sns2	95	94	6.0000000	10.000000	8.0000000	8.0152408	8.0344076	0.152559	0.76	0.0037462	0.09	176.60	1.05		
101	lvcc_sns2	95	92	-8.0000000	-4.0000000	-6.008752	5.995336	-6.008447	-0.76	0.0037462	0.09	130.24	1.05			
102	lact_vdd	95	95	1.3000000	2.3000000	1.7898986	1.7997333	1.7992352	-0.15	0.0001363	0.01	245.12	1.05			
103	lvcc_err	95	94	-0.3000000	0.2000000	-0.087595	0.0394073	0.0025556	20.10	0.0037462	0.75	1221.36	1.05			
104	lvcc_err	95	92	-0.2000000	0.3000000	0.012476	0.0246644	0.0150531	-13.98	0.0027130	0.54	17.77	1.05			
105	lvcc_err	95	95	-0.0540000	0.0540000	-0.0010513	-0.0010513	-0.0010513	-1.12	0.0001363	0.13	4.06	2.11			
106	lvcc_icc	95	91	0.4000000	1.5000000	0.5746000	0.7639000	0.6757923	-49.86	0.0447130	2.22	3.76	1.05			
107	lvcc_iee	95	91	-1.5000000	-0.4000000	-1.124900	-0.9970000	-0.52923	-18.71	0.0197035	1.79	7.56	3.16			
108	lvcc_idd	95	91	-0.0500000	0.0500000	0.0155030	0.0165251	0.0160833	32.17	0.0002514	0.25	44.98	2.11			
109	lvcc_power	95	89	6.0000000	15.000000	10.950113	12.540612	11.764489	28.10	0.2654412	2.95	4.06	2.11			
110	lvcc_sns1	95	92	6.0000000	10.000000	8.0006723	8.0485315	8.0263559	1.18	0.0090414	0.24	70.07	2.11			
111	lvcc_plane	95	93	6.0000000	10.000000	8.0628801	8.1034517	8.0077559	3.89	0.0079888	0.20	80.21				

Exhibit 5, p. 2 of 5

Valid	Stat	Test Limits		Statistic Data Range		Mean	Units	Pos %Limit	Units	Std Dev	CPK	% Exe Fail	Notes	
		Qty		Min	Max									
	Test Name	Tests												
Numb														
112	l12_1)vee_sns1	95	92	-8.000000	-4.000000	-6.117024	-5.964578	-6.052285	-6.61	0.0210411	0.53	30.86	2.11	
113	l13_1)vee_plane	95	93	-8.000000	-4.000000	-6.220200	-6.058495	-6.132995	-6.65	0.0173310	0.43	35.91		
114	l14_1)md_sense	95	92	-0.500000	0.500000	-0.0405250	-0.0112598	-0.0278874	-5.60	0.0039322	0.39	40.02	1.05	
115	l15_1)md_sense	95	92	-0.500000	0.500000	-0.0400000	-0.0112598	-0.0280442	-5.60	0.003874	0.39	40.64	1.05	
116	l16_1)edge_sense	95	91	-0.500000	0.500000	-0.0400000	-0.0112598	-0.0255936	-5.47	0.0027203	0.27	57.71		
117	l17_1)ncy7	95	93	-0.500000	0.500000	-0.0203355	-0.0106759	-0.018788	-2.01	0.0018788	0.19	86.92	1.05	
118	l18_1)Ring_Gnd	95	95	-0.500000	0.500000	-0.0207060	0.0033336	0.029818	0.60	0.0001778	0.01	1406.97		
130	l30_IDLE_P1	95	92	0.0004500	0.0150000	0.0007562	0.008499	0.008314	-27.36	1.11e-05	1.06	11.45	3.16	
131	l31_IDLE_P2	95	94	0.0004500	0.0150000	0.0008570	0.008343	0.008343	-26.79	1.327e-05	1.26	9.65	1.05	
132	l32_IDLE_N1	95	93	-0.015000	-0.004500	-0.008569	-0.008031	-0.008555	-22.77	1.537e-05	1.56	8.25	1.05	
133	l33_IDLE_N2	95	90	-0.015000	-0.004500	-0.008920	-0.007551	-0.008525	23.33	1.734e-05	1.65	7.74	3.16	
134	l34_T_SLRD1	95	91	0.0004000	0.0300000	0.0017936	0.019061	0.018729	13.30	2.134e-05	0.82	17.61	2.11	
135	l35_T_SLRD2	95	91	0.0004000	0.0300000	0.0013399	0.022120	0.020325	25.58	3.321e-05	1.28	9.71	1.05	
136	l36_T_SLF1	95	92	-0.0300000	-0.0040000	-0.019231	-0.017141	-0.013377	-10.59	3.145e-05	1.21	12.32	1.05	
137	l37_T_SLF2	95	91	-0.0300000	-0.0040000	-0.019019	-0.0017189	-0.016322	-10.17	2.959e-05	1.14	13.16	1.05	
138	l38_IMON_DC	95	94	0.0050000	0.0200000	0.0113363	0.0014984	0.0014203	-15.93	2.668e-05	2.67	5.25	1.05	
139	l39_IMON_AC	95	92	0.0050000	0.0200000	0.013491	0.0014502	0.014119	-17.61	1.762e-05	1.76	7.79	3.16	
140	l40_T_DIG_DC_MON	95	93	-0.0020000	-0.0010000	-0.014400	-0.013020	-0.014020	19.60	2.228e-05	2.22	6.04	2.11	
160	l60_AB1_VL_FUNCN1	95	88	-1.500000	-0.8000000	-1.188696	-1.148132	-1.147430	-6.57	0.007413	1.01	15.41	6.32	
161	l61_AB1_VL_OFSS	95	88	-0.4000000	0.2000000	-0.205445	-0.1650396	-0.1911870	-30.40	0.0073228	1.22	9.51	4.21	
162	l62_AB1_VL_FUNCP3	95	87	-2.8000000	3.5999999	3.0432317	3.0873256	3.0616252	-34.59	0.0085048	1.06	10.25	6.32	
163	l63_AB1_VH_FUNCN1	95	87	-1.2000000	-0.4000000	-0.6161010	-0.5578843	-0.5851599	53.87	0.0154949	1.94	3.97	6.22	
164	l64_AB1_VH_OFSS	95	90	-0.2000000	0.4000000	0.2066211	0.3249375	0.2952538	66.17	0.0180570	3.01	1.87	5.26	
165	l65_AB1_VH_FUNCP4	95	86	3.7000000	4.5999999	4.1005464	4.2542481	4.2278857	17.31	0.0210521	2.33	5.91	8.42	
170	l70_AB2_VL_FUNCN1	95	83	-1.500000	-0.8000000	-1.188696	-1.148132	-1.147430	-6.57	0.0059547	0.85	18.31	8.42	
171	l71_AB2_VL_OFSS	95	83	-0.4000000	0.2000000	-0.2035630	-0.1702179	-0.1899934	-30.00	0.0053909	1.07	10.95	10.53	
172	l72_AB2_VL_FUNCP3	95	83	-2.8000000	3.5999999	3.0366852	3.0908563	3.0637746	-34.06	0.0073855	0.92	11.91	11.58	
173	l73_AB2_VH_FUNCN1	95	87	-1.2000000	-0.4000000	-0.6161010	-0.5578843	-0.5851599	62.81	0.0241635	3.02	2.05	7.37	
174	l74_AB2_VH_OFSS	95	87	-0.2000000	0.4000000	0.2288251	0.3677839	0.3337845	77.93	0.0253665	4.23	5.91	8.42	
175	l75_AB2_VH_FUNCP4	95	84	3.7000000	4.5999999	4.1061464	4.2542481	4.2278857	17.31	0.0210521	2.33	5.91	7.37	
180	l80_ROOT_1_VL+50	95	92	35.000000	55.000000	40.000000	40.452862	40.492942	40.897110	8.97	2.1174841	10.59	1.43	4.21
181	l81_ROOT_1_VH-50	95	92	35.000000	55.000000	40.000000	40.580833	40.824238	45.845787	8.46	1.8597041	9.56	1.64	3.16
182	l82_ROOT_2_VL+50	95	94	35.000000	55.000000	39.7751318	47.632523	44.741272	-2.59	1.1311038	3.02	2.87	1.05	
183	l83_ROOT_2_VH-50	95	92	35.000000	55.000000	44.400005	47.776886	45.538006	5.38	0.8413368	4.21	3.75	3.16	
2000	Part_ID	95	95	999	0	1.0000000	924	0.0000000	-25.79	319.51089	31.98	0.39		
2130	l2130_IDLE_P1	95	91	0.0004500	0.0055000	0.0005000	0.0005000	0.0005000	26.24	0.0206646	2.30	5.35		
2131	l2131_IDLE_P2	95	94	0.0004500	0.0055000	0.0004755	0.0004999	0.0004999	14.84	1.96e-06	1.96	7.24		
2132	l2132_IDLE_N1	95	94	-0.0005500	-0.0004500	-0.0004999	-0.0004661	-0.0004661	-20.61	6.095e-06	6.10	2.17		
2133	l2133_IDLE_N2	95	92	-0.0005500	-0.0004000	-0.0004500	-0.0004500	-0.0004500	15.85	7.16e-06	7.52	1.81		
2134	l2134_T_SLRD1	95	88	0.0004000	0.0007000	0.0007000	0.0005090	0.0005090	20.71	6.986e-06	6.99	1.89		
2135	l2135_T_SLF2	95	92	0.0004000	0.0007000	0.0003106	0.0003106	0.0003106	-17.78	8.05e-06	2.67	5.14		
2136	l2136_T_SLF1	95	92	-0.0007000	-0.0004000	-0.0005249	-0.0004721	-0.0004721	-24.72	1.085e-05	1.97	7.37		
2137	l2137_T_SLF2	95	93	-0.0007000	-0.0004000	-0.0005300	-0.0004755	-0.0004755	3.62	0.0026217	0.07	253.72	1.05	
2180	l2180_ROUT_1	95	89	48.000000	52.000000	49.892139	50.347202	49.962582	27.47	1.284e-05	4.28	2.83	2.11	
2181	l2181_ROUT_2	95	93	48.000000	52.000000	49.892139	50.347202	49.962582	-1.87	0.0644347	1.61	10.15		
3100	l3100_1)vee_sns2	95	93	6.0000000	10.000000	8.066684	8.0216970	8.013623	4.35	0.1012987	2.53	6.29		
3101	l3101_1)vee_sns2	95	92	-8.0000000	-4.000000	-6.08360	-5.995257	-6.004480	-1.20	5.872e-05	0.07	229.04		
3102	l3102_1)act_vdd	95	93	-1.5000000	2.3000000	1.7995340	1.7995623	-0.09	0.0003115	0.01	1492.93			
3103	l3103_1)vee_err	95	93	-0.3000000	0.2000000	0.0981320	0.0666937	-0.0666937	19.74	0.028898	0.58	23.14		
3104	l3104_1)max_1idd	95	92	-0.2000000	0.3000000	0.0116401	0.0247202	0.0155196	-13.79	0.026217	0.52	27.40		
3105	l3105_1)vee_err	95	95	-0.0540000	0.0540000	-0.006590	-0.001698	-0.0004376	-0.81	0.0001115	0.10	160.07		
3106	l3106_1)max_icc	95	89	0.4000000	1.5000001	0.5102000	0.6094000	0.5482809	1.75	0.0072449	0.18	90.66		
3107	l3107_1)max_iee	95	93	-8.0000000	-4.000000	-6.125419	-6.075070	-6.075070	3.67	0.0069605	0.17	92.26		
3108	l3108_1)max_1idd	95	93	-8.0000000	-4.000000	-6.194386	-6.056848	-6.127488	4.02	0.0146468	1.33	12.01		
3109	l3109_1)max_power	95	89	6.0000000	15.000000	9.4597561	10.842550	9.9011985	-11.31	0.0202607	43.35	2.11		
3110	l3110_1)vee_sns1	95	92	6.0000000	10.000000	8.0203648	8.0562267	8.0506609	2.25	6.56	1.05			
3111	l3111_1)vee_plane	95	93	6.0000000	10.000000	8.0631237	8.0963334	8.0734377	1.75	0.0072449	0.18	90.66		
3112	l3112_1)vee_sns1	95	92	-8.0000000	-4.000000	-6.125419	-6.075070	-6.075070	3.67	0.0069605	0.17	92.26		
3113	l3113_1)vee_plane	95	93	-8.0000000	-4.000000	-6.194386	-6.056848	-6.127488	4.02	0.0146468	1.33	12.01		
3114	l3114_1)gd_sense	95	92	-0.5000000	0.5000000	-0.0398973	-0.0398973	-0.0398973	-5.54	0.0039201	0.39	40.48		
3130	l3130_IDLE_P1	95	90	0.0004300	0.0005500	0.0005026	0.0005129	0.0005129	20.67	2.02e-06	2.02	1.05		

Numb	Test Name	Tests	Qty	Test Limits		Statistic Data Range		Units	Pos	Limit	Units	%Limit	Std. Dev	CPK	% Exe Fail	Notes
				Min	Max	Min	Max									
3131	IDLE_P2	95	94	0.0004500	0.0005500	0.0004780	0.0005295	0.0004929	-14.15	7.181e-06	7.18	1.99	1.05			
3132	IDLE_N1	95	93	-0.0005500	-0.0004500	-0.0005018	-0.0004677	-0.0004923	15.32	7.752e-06	7.75	1.62	2.11			
3133	IDLE_N2	95	91	-0.0005500	-0.0004500	-0.0005019	-0.0004749	-0.0004917	16.52	7.005e-06	7.00	1.99	4.21			
3134	T_SLRD1	95	89	0.0004000	0.0004500	0.0007000	0.0005141	0.0005594	0.0005296	-13.59	9.201e-05	3.07	4.70	3.16		
3135	T_SURD2	95	92	0.0004000	0.0004500	0.0007000	0.0003091	0.0005481	-1.24	5.897e-05	19.66	*	0.84	7.37		
3136	T_SLF1	95	93	-0.0006000	-0.0004000	-0.0005253	-0.0004723	-0.0005130	-13.03	1.083e-05	5.45	2.66	2.11			
3137	T_SLF2	95	93	-0.0006000	-0.0004000	-0.0005277	-0.0004752	-0.0005081	-8.14	1.296e-05	6.48	2.36	2.11			
3138	IMON_DC	95	94	0.0012000	0.0018000	0.0018000	0.0013361	0.0014881	0.0014204	-26.53	2.671e-05	4.45	2.75	1.05		
3139	IMON_AC	95	92	0.0012000	0.0018000	0.0018000	0.0013489	0.0014508	0.0014123	-29.22	2.676e-05	2.95	4.00	3.16		
3140	DIG_IMON	95	93	-0.0017500	-0.0012500	-0.0014400	-0.0013020	-0.0014021	39.14	2.223e-05	4.45	2.28	2.11			
3151	T_SURD1_100	95	90	0.0001500	0.0005000	0.0003875	0.0004508	0.0004005	43.17	1.292e-05	3.69	2.57	4.21			
3152	T_SLF1_100	95	93	-0.0006000	-0.0004000	-0.0005250	-0.0004722	-0.0005129	-12.89	1.083e-05	5.43	2.68	2.11			
3153	T_SURD2_100	95	93	0.0001500	0.0005000	0.0005000	0.0015e-08	0.0002897	-20.18	6.972e-05	19.92	*	0.77	7.37		
3154	T_SLF2_100	95	93	-0.0006000	-0.0004000	-0.0005275	-0.0004751	-0.0005080	-8.00	1.279e-05	6.39	2.40	2.11			
3155	T_SURD1_I64	95	89	0.0005000	0.0009500	0.0006370	0.0007647	0.0006616	-28.18	1.104e-05	2.45	2.28	3.16			
3156	T_SLF1_I64	95	93	-0.0006000	-0.0004000	-0.0005252	-0.0004724	-0.0005130	-13.03	1.097e-05	5.48	2.64	2.11			
3157	T_SURD2_I64	95	93	0.0005000	0.0009500	0.0005150	0.0010172	0.0008097	37.66	7.347e-05	16.33	*	0.64	5.26		
3158	T_SLF2_I64	95	93	-0.0006000	-0.0004000	-0.0005276	-0.0004750	-0.0005083	-8.35	1.317e-05	6.59	2.32	2.11			
3159	ABI_VL_FUNCN1	95	88	-1.3000000	-0.7000000	-1.0156931	-0.9909786	-1.0047229	-1.58	0.0047940	0.80	20.53	5.26			
3161	ABI_VL_OFSS	95	89	-0.3000000	0.2000000	-0.0255393	-0.0233154	-0.0152612	13.90	0.0044245	0.88	16.22	5.26			
3162	ABI_VL_FUNCNP3	95	88	3.0000000	3.5999999	3.2495792	3.2735875	3.2591386	-13.62	0.0042936	0.72	6.32	6.32			
3163	ABI_VL_FUNCN1	95	87	-1.1000000	-0.6000000	-0.7897310	-0.7573274	-0.7736550	42.12	0.0044150	1.07	9.02	5.26			
3164	ABI_VH_OFSS	95	88	-0.2000000	0.3000000	0.1007798	0.1373418	0.1157227	26.29	0.0067261	1.35	9.13	5.26			
3165	ABI_VH_FUNCNP4	95	87	3.7000000	4.3000002	4.0644555	4.0912886	4.0760007	25.33	0.0065416	1.09	11.41	7.37			
3170	AB2_VL_FUNCN1	95	88	-1.3000000	-0.7000000	-1.047391	-0.9819558	-1.009852	-3.28	0.0071838	1.20	13.46	5.26			
3171	AB2_VL_OFSS	95	88	-0.3000000	0.2000000	-0.056091	-0.0507997	-0.052638	11.89	0.0068148	1.36	10.77	6.32			
3172	AB2_VL_FUNCNP3	95	88	3.0000000	3.5999999	3.2188234	3.2793266	3.2540638	-15.31	0.0063338	1.06	13.37	6.32			
3173	AB2_VH_FUNCN1	95	87	-1.2000000	-0.6000000	-0.8338250	-0.6926771	-0.7403099	53.23	0.0216058	3.60	2.16	8.42			
3174	AB2_VH_OFSS	95	87	-0.2000000	0.3000000	0.0560582	0.1956369	0.1481818	39.27	0.0217866	4.36	2.32	7.37			
3175	AB2_VH_FUNCNP4	95	88	3.7000000	4.3000002	4.0207534	4.1903820	4.1083293	36.11	0.0219003	3.65	2.92	6.32			

NOTES:

- There are no test limits for this Parameter in the Limit File. The CpK is calculated using the limits found in the File Analyzed.
- Asymmetrical Guardband limits. The CpK refers to the high limit only.
- Asymmetrical Guardband limits. The CpK refers to the Low limit only.
- No test limits. The CpK, Mean position and Std. Dev. Limit Span could not be calculated for this test.
- Alarms detected on 1 or more parts. These parts are not included in the 'Valid Tests' quantity or the statistics.
- This data represents the statistics for one specific test site.

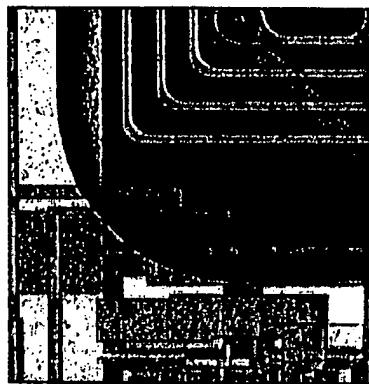
Parameter	637980	637980	637980.5	637980	637980	637980	COMBINED
							LOTS
Qty of Parts Tested	24	24	3	20	24	95	
Qty of Parts PASS	17	19	2	15	8	61	
Yield	70.83%	79.17%	66.67%	75.00%	33.33%	64.21%	
Total Devices Binned	24	24	3	20	24	95	
Bin 1	17	19	2	15	8	61	
Bin 11	0	0	0	0	1	1	
Bin 97	7	5	1	5	15	33	
	29.17%	20.83%	33.33%	25.00%	62.50%	34.74%	

DATE: October 12th, 2000
TO: Rick Morrison
FROM: Justin Borski

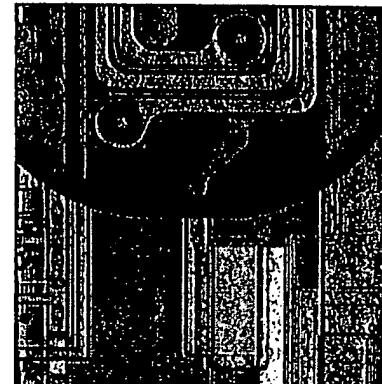
SUBJ: First T-COIL PC-10 Wafer Delivered!

Rick, below please find information pertaining to each wafer delivered in this shipment. There are VMI wafer defect maps associated with each T-COIL product wafer included in this shipment. Prior to post-wafer assembly, these wafers should be inspected to ensure selection of functional die based on the VMI maps. Engineering data and items of interest include:

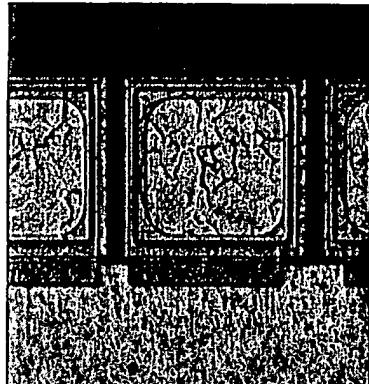
- Wafers 02B5 and 2111 (non-int.) have AMS-deposited encapsulation of 0.5 μ m Al₂O₃. The aluminum oxide has been reactively etched away from on top of all but two thin-film trim resistors. The two trim resistors effected are shown in picture (1).
- Wafers 06D6 and 2112 (non-int.) DO NOT have AMS encapsulation.
- Shown below are some relevant pictures of design and/or device issues to be aware of during packaging and test:



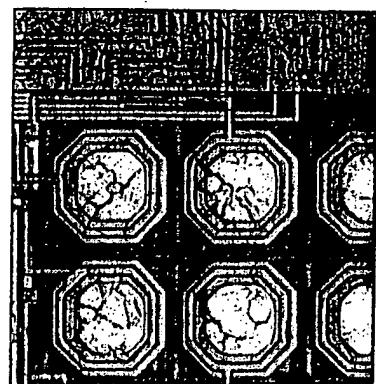
1.) Thin-film trim resistors covered by insulator



2.) Uncovered thin-film trim resistors, wafer 02B5



3.) Non-conductive ring area on aluminum bond pad, wafer 02B5



4.) Probe-points area reduction; wafer 06D6 conductive, wafer 02B5 non-conductive



- Key measurement data taken during AMS post-processing:

Ruthenium Barrier

Rs (ohms/sq)	Non-uniformity (%)
1.61	0.3

Insulator Thickness

Wafer ID	Thickness Mean (μm)	Thickness Range (μm)
2111	7.5	0.2
2112	7.7	0.1

Copper Coil Thickness

Wafer ID	Thickness Mean (μm)	Thickness Range (μm)
2111	5.6	0.5
2112	6.3	0.5
02B5	6.7	0.6
06D6	7.0	0.5

Aluminum Oxide Encapsulation

Thickness Mean (μm)	Non-uniformity (%)
4980	1.5

BOX 1, 4 T-COIL WAFERS

SLOT	WAFER ID	LOT - DESCRIPTION
25		
24		
23		
22		
21		
20		
19		
18		
17		
16		
15		
14		
13		
12		
11		
10	06D6	TCL-002
9		
8	2112	TCL-002
7		
6		
5		
4	02B5	TCL-002
3		
2	2111	TCL-002
1		

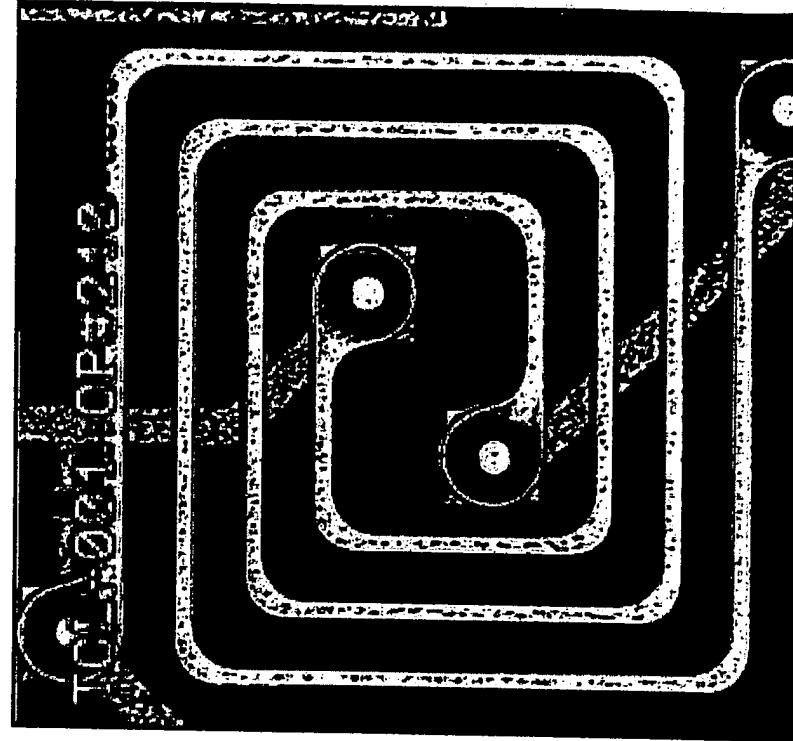
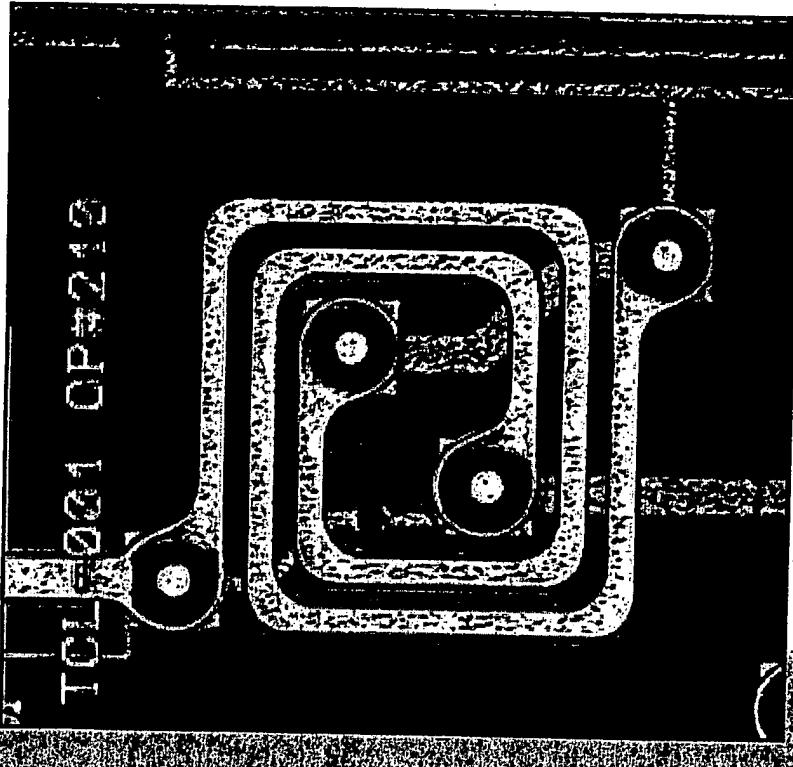
Regards,

Justin C. Borski
Advanced MicroSensors Inc.

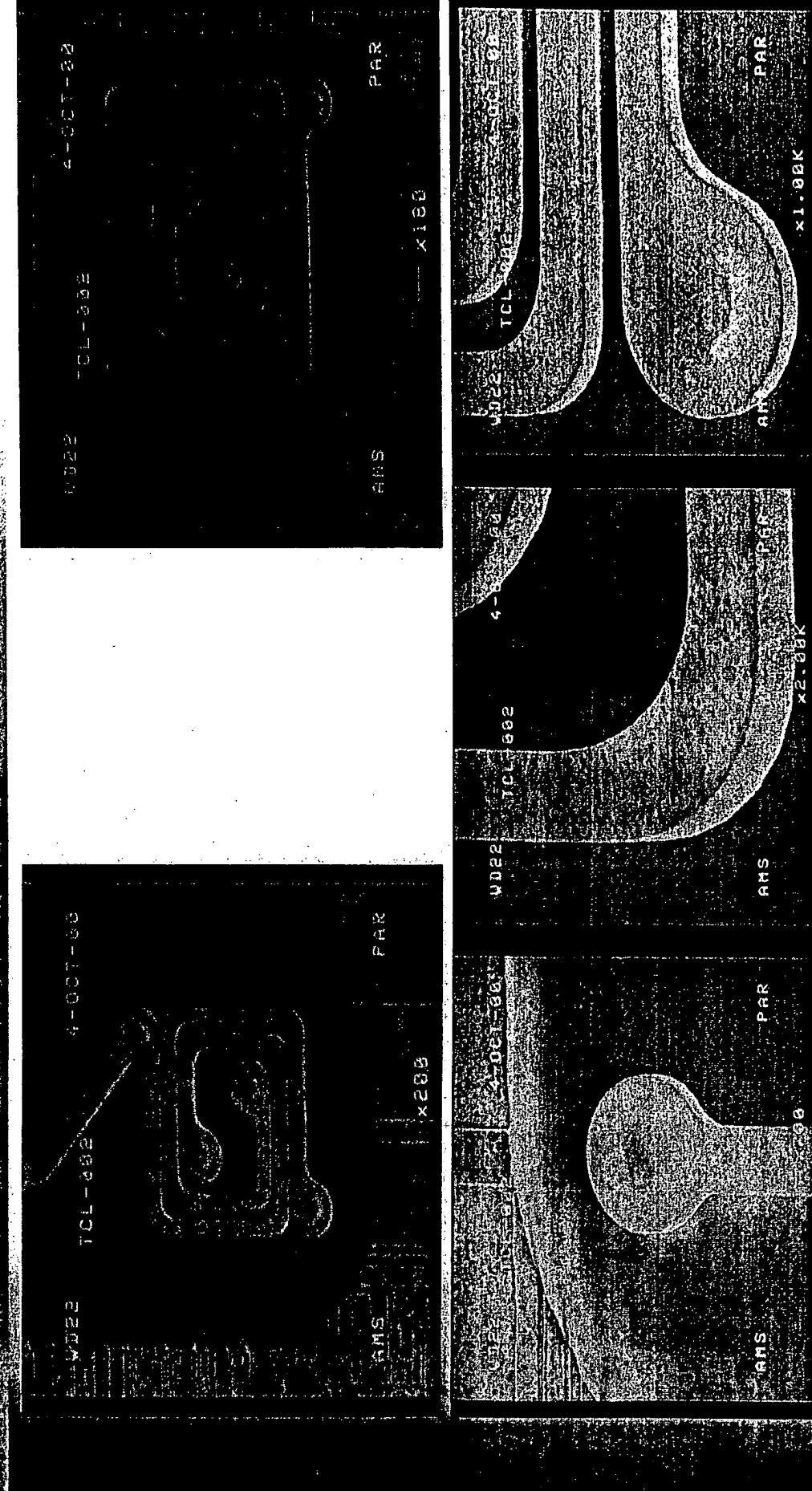
Advanced MicroSensors Confidential

Exhibit 6, p. 2 of 2

First On-Chip T-Coils (1)



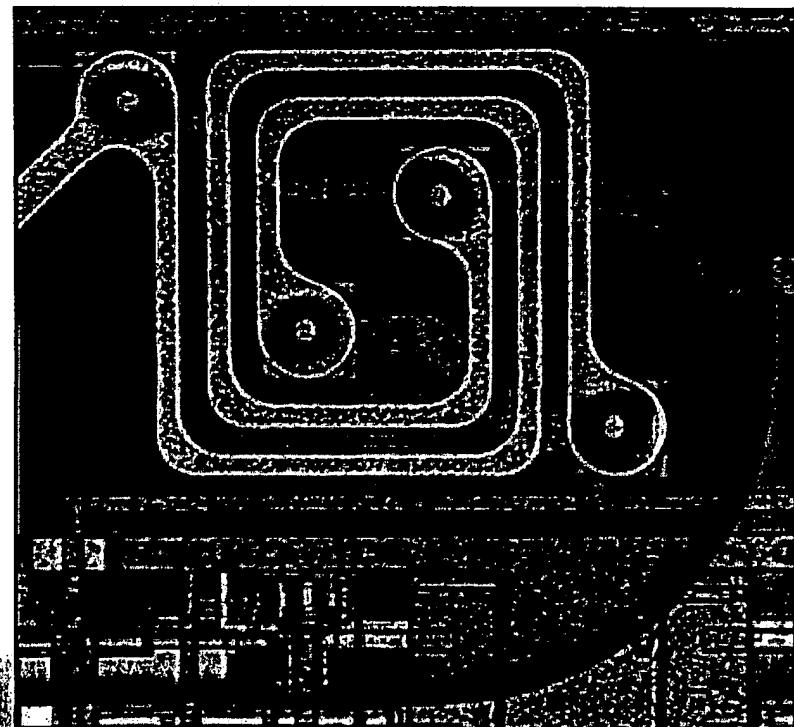
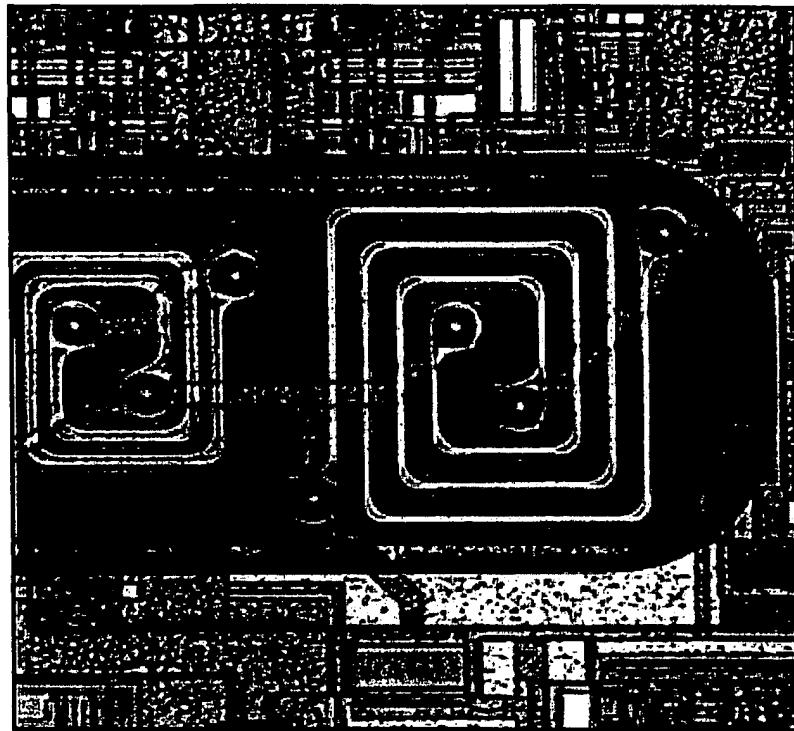
First On-Chip T-Coils (2)



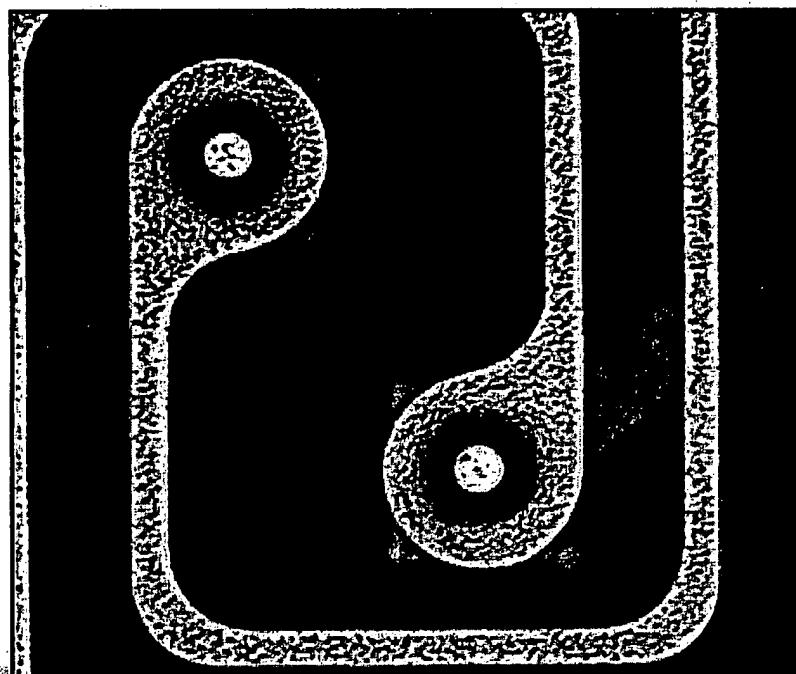
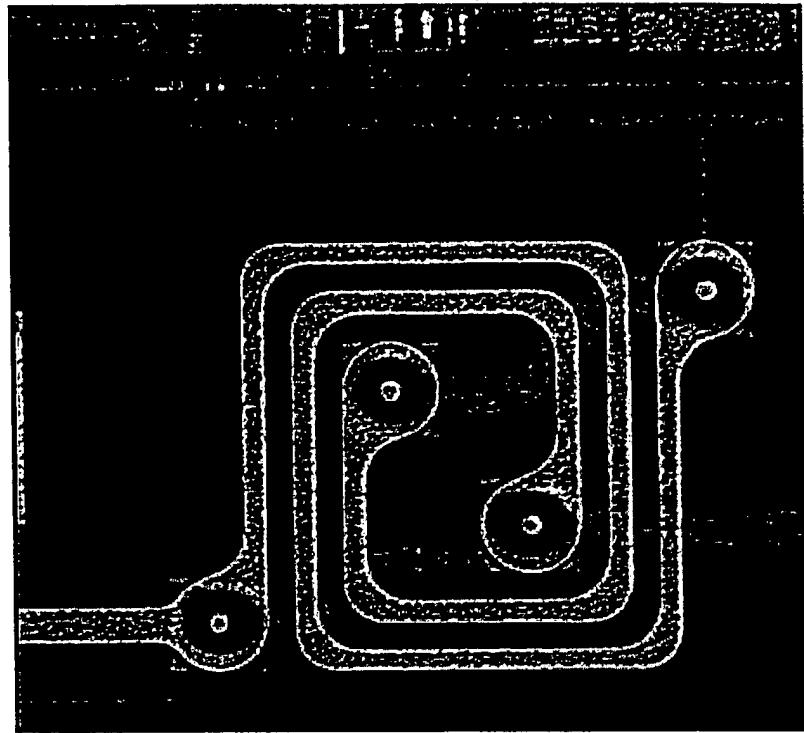
ADI Proprietary
2

**ANALOG
DEVICES**

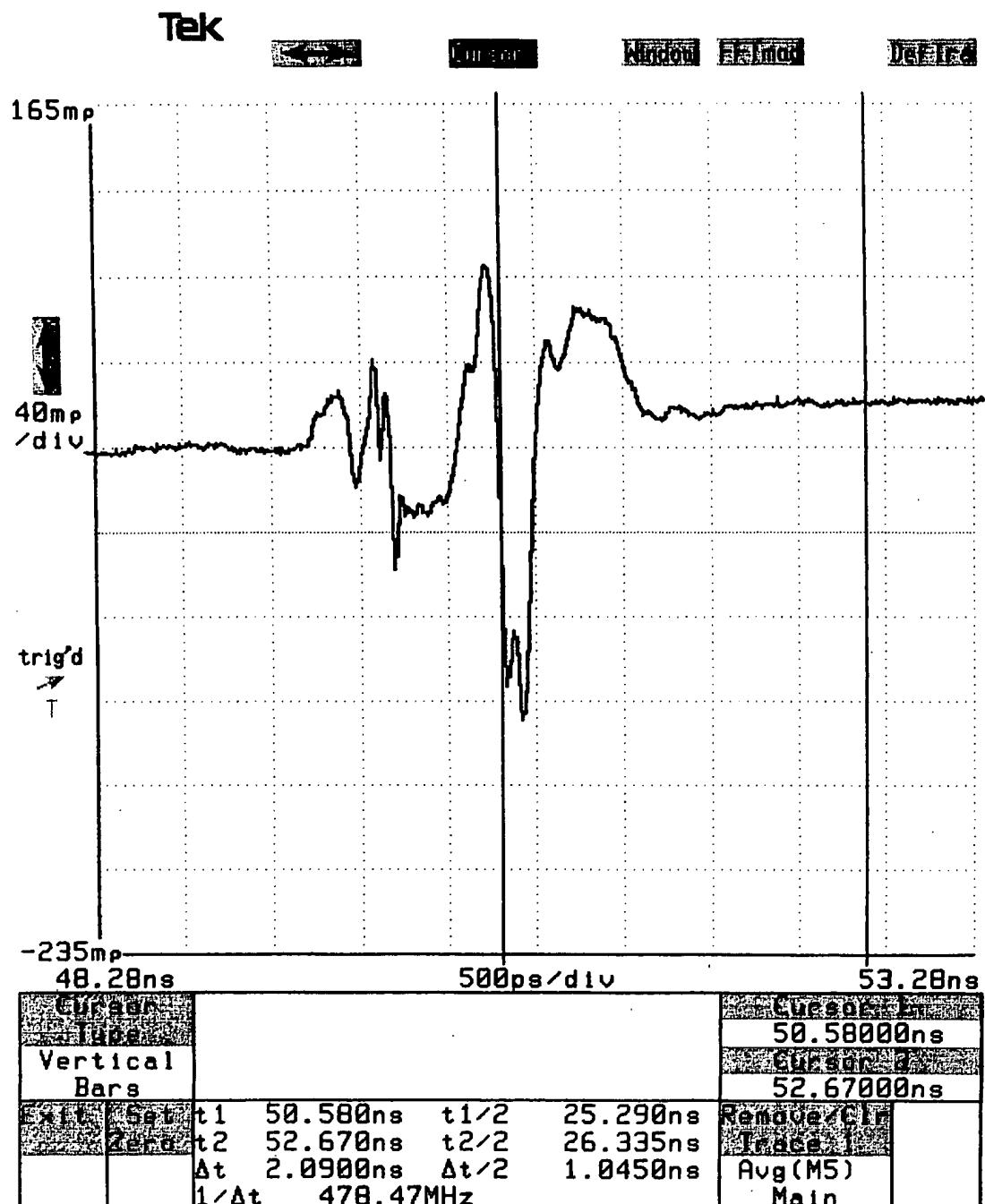
First On-Chip T-Coils (3)



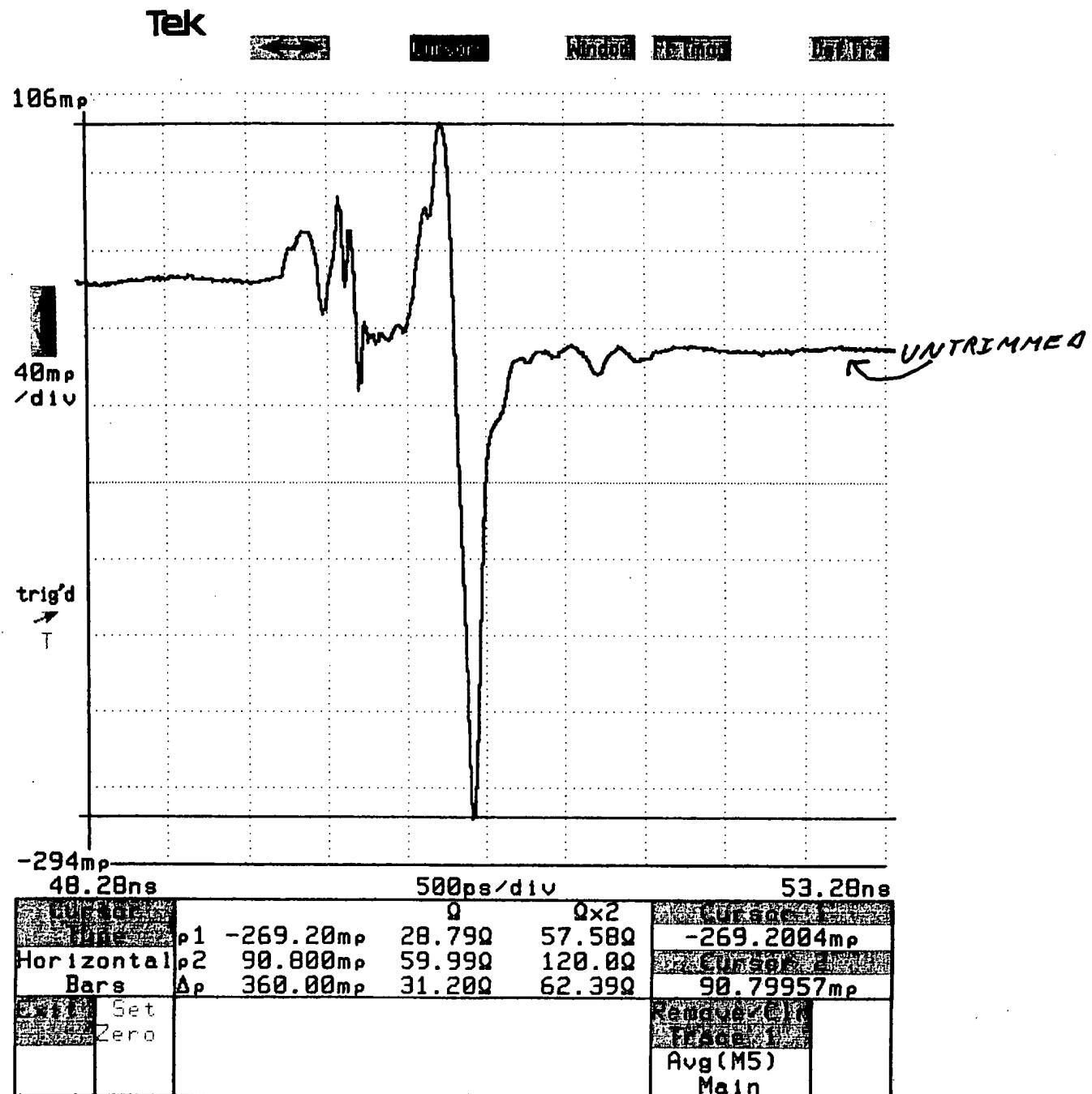
First On-Chip T-Coils (4)



11801C DIGITAL SAMPLING OSCILLOSCOPE
date: 17-OCT-00 time: 10:02:59



11801C DIGITAL SAMPLING OSCILLOSCOPE
date: 18-OCT-00 time: 14:46:24



PIN 1

PROBES DOWN
POWER ON
NOT WITHOUT T COILS

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